X-721-67-603

NASA TM X- 63070

DATA FORMAT CONVERTER

GPO PRICE $ _____

CFSTI PRICE(S) $ _____

Hard copy (HC) 3.00

Microfiche (MF) .65

ff 653 July 65

N68-15745

(ACCESSION NUMBER)	(THRU)
55 (PAGES)	1 (CODE)
TMX-63070 (NASA CR OR TMX OR AD NUMBER)	08 (CATEGORY)

FACILITY FORM 602

DECEMBER 1967

GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND

X-721-67-603

DATA FORMAT CONVERTER

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and
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Sounding Rocket Instrumentation Section

December 1967

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

ABSTRACT

The Data Format Converter accepts nine-bit parallel binary data at a 5-kilohertz rate, combines the data with time readings, and records them on a one-half inch 7 track computer-compatible binary tape. The converter is a part of a pulse position modulation (PPM) telemetry system, designed by the Sounding Rocket Instrumentation Section of Goddard Space Flight Center, which is used extensively for sounding rocket flights. The computer compatible tape can be processed by a computer to analyze the results of rocket flight experiments and instrumentation performance.

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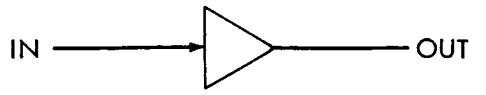
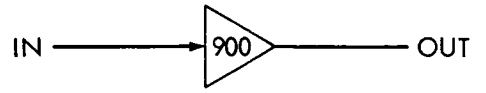
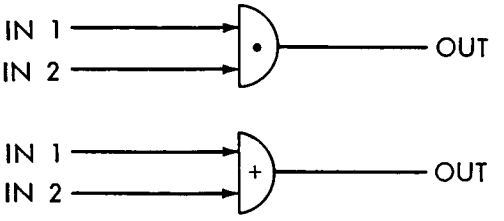
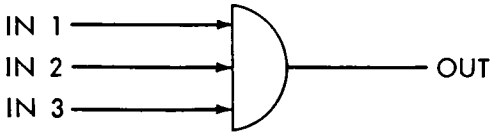
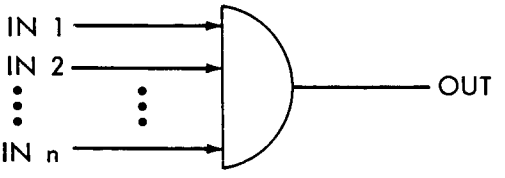
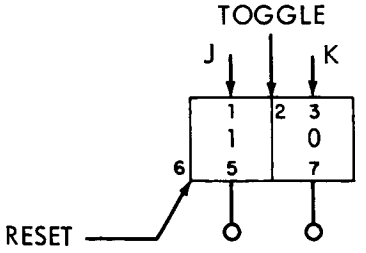
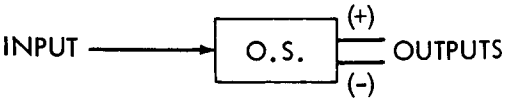
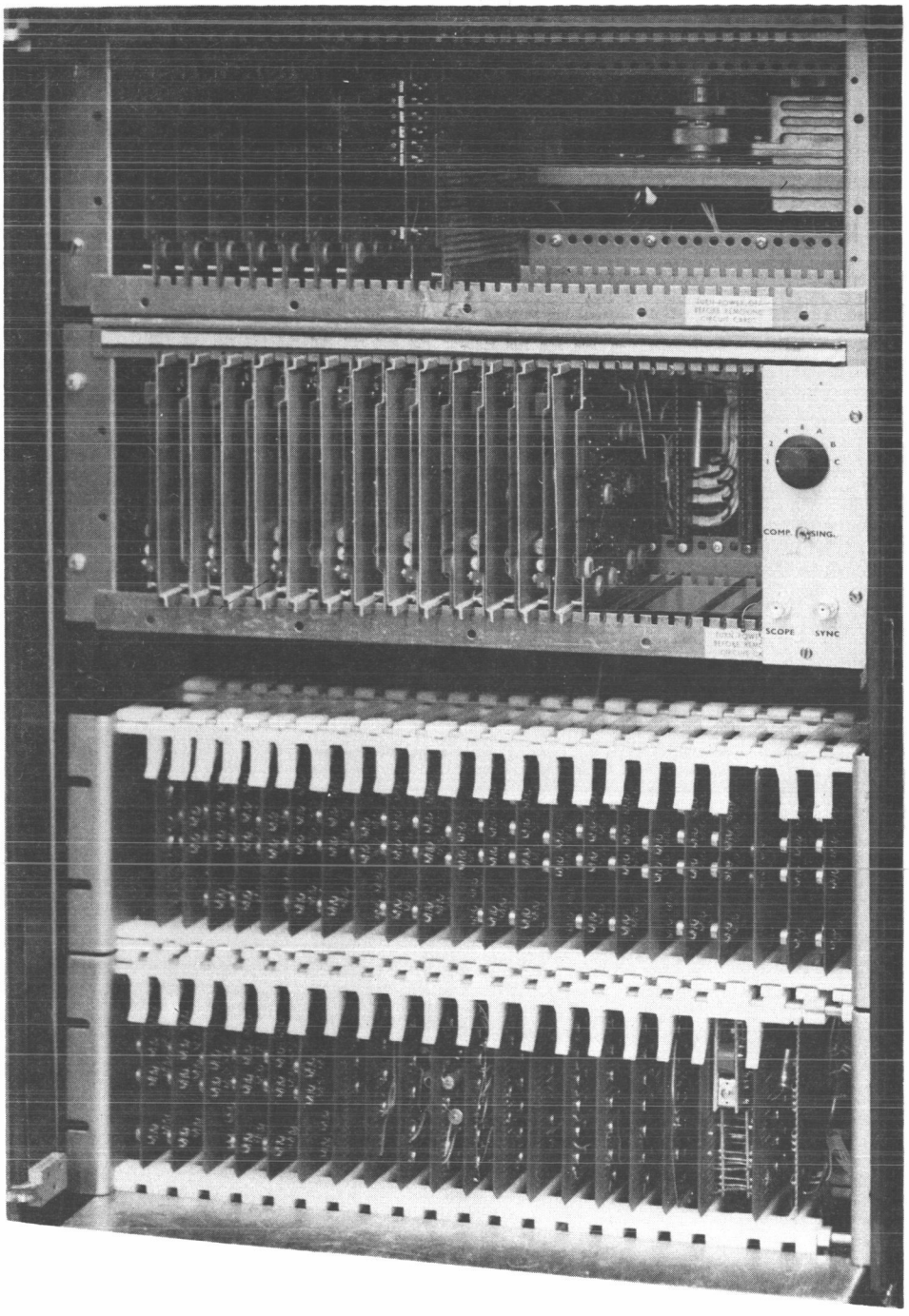
ILLUSTRATIONS

TABLE

SYMBOLS USED IN DIAGRAMS

SYMBOL	EXPLANATION
	INVERTER—Can be 1/2 of an FμL 914 gate or it could be a single transistor inverter
	FμL 900 high fan-out inverter
	Both of these symbols represent 1/2 of the FμL 914 "NAND" gate can ; the dot implies that the gate is functioning as an "AND" gate for negative signals; the + sign indicates functioning as an "OR" gate for positive signals
	This is the FμL 903 - 3 input "NAND" gate ; a dot or a + indicates "AND" or "OR", respectively
	A gate with 4 or more inputs is simply a combination of parallel FμL 914's
	Diodes are blackened in to prevent any possible misinterpretation as an inverter
	This is the symbol for the FμL 923 J-K flip-flop. Output 5 is +3V after a reset. If either pins 1,3, or 6 are not shown this omission automatically implies that the missing pin is grounded.
	This is the symbol for a one-shot multivibrator (generally made from a FμL 914 can). The (+) output is a +3V signal the (-) output is a +3V to gnd signal



Frontispiece. Data Format Converter in Beltsville PPM Ground Station

DATA FORMAT CONVERTER

INTRODUCTION

The Sounding Rocket Instrumentation Section of Goddard Space Flight Center designed and implemented a pulse position modulation (PPM) telemetry system that is used extensively for sounding rocket flights. Figure 1 shows a block diagram of the system. The system is used both for real time missions in the field, and at the test or assembly station, where the experiments and rocket instrumentation are integrated and prepared for flight. The PPM telemetry system is divided into two major systems: one is the airborne PPM system aboard the sounding rocket, and the other is a PPM ground station system that receives and records the data transmitted by the airborne system.

System Description

This report deals exclusively with the Data Format Converter of the PPM ground station. The Data Format Converter accepts nine-bit parallel binary data at 5 kilohertz, combines the data with a serial time code, and yields a one-half inch computer-compatible binary tape. This tape, with its compacted data, is now ready to be fed into a computer to analyze the results of the rocket flight experiments and of the instrumentation performance. A one-inch tape on the PPM ground station transfers the input data, that is recorded from the sounding rocket, into the Data Format Converter. A 7-track binary recorder (one-half inch tape) is used to record the computer-compatible output data.

The telemetry data in 9 bit parallel binary words and a 36-bit NASA unmodulated serial time code are recorded in real time on the one-inch 16-track tape recorder at the PPM Telemetry ground receiving station. The telemetry system can be used at three different data sampling rates; 5 kilohertz, 10 kilohertz, or 20 kilohertz. When recording the data, the tape recorder is run at 15 inches per second, 30 inches per second, or 60 inches per second, respectively depending on the sampling rate. When playing back the tape, only 15 inches per second is used so that the data is always reproduced at a 5 kilohertz rate, although the time code will vary.

DATA FORMAT CONVERTER SUBSYSTEMS

The Data Format Converter consists of the four following basic subsystems (Figure 2): time code; data memory; format gating; and tape unit and writing control.

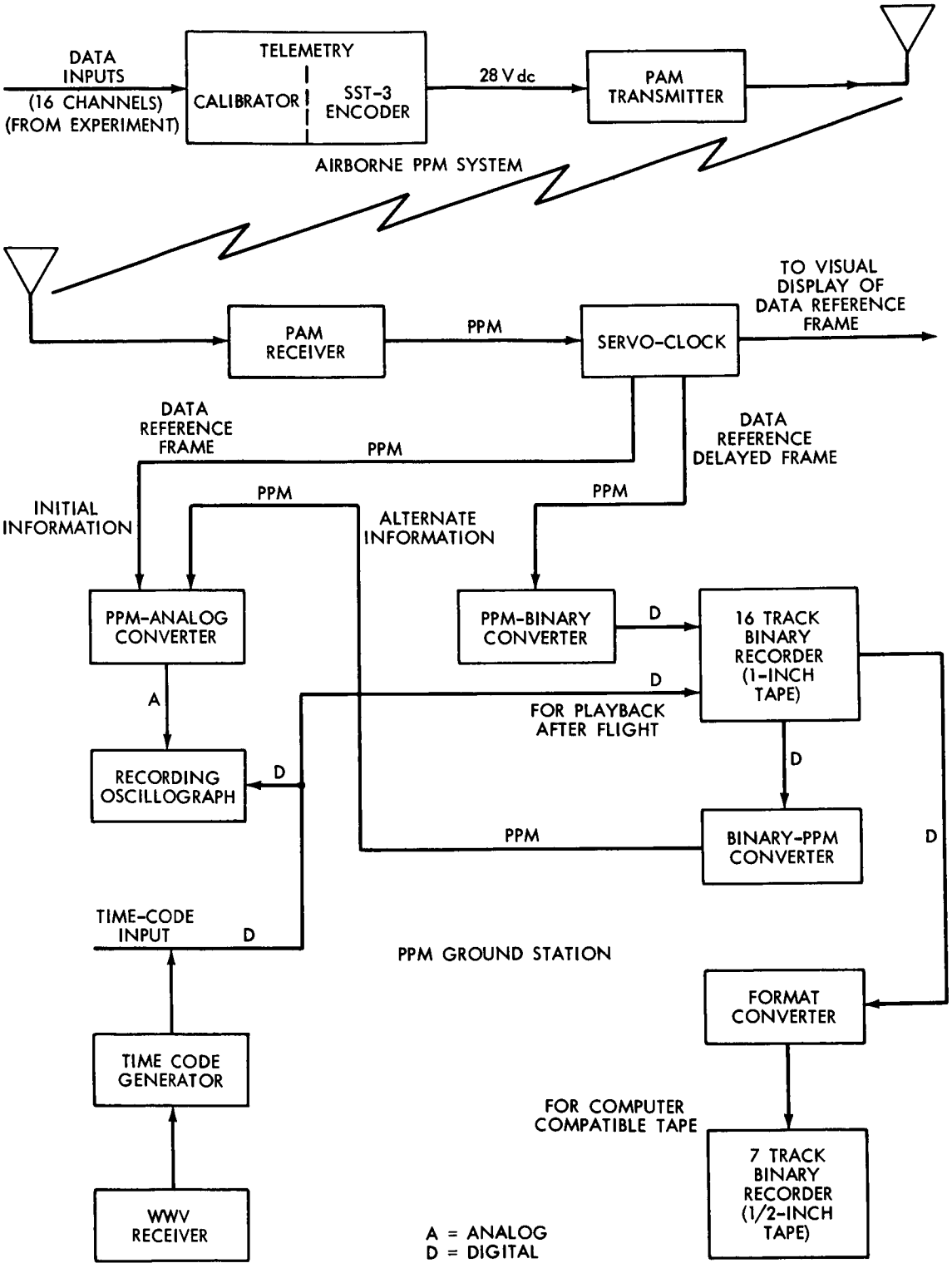


Figure 1. PPM Telemetry System

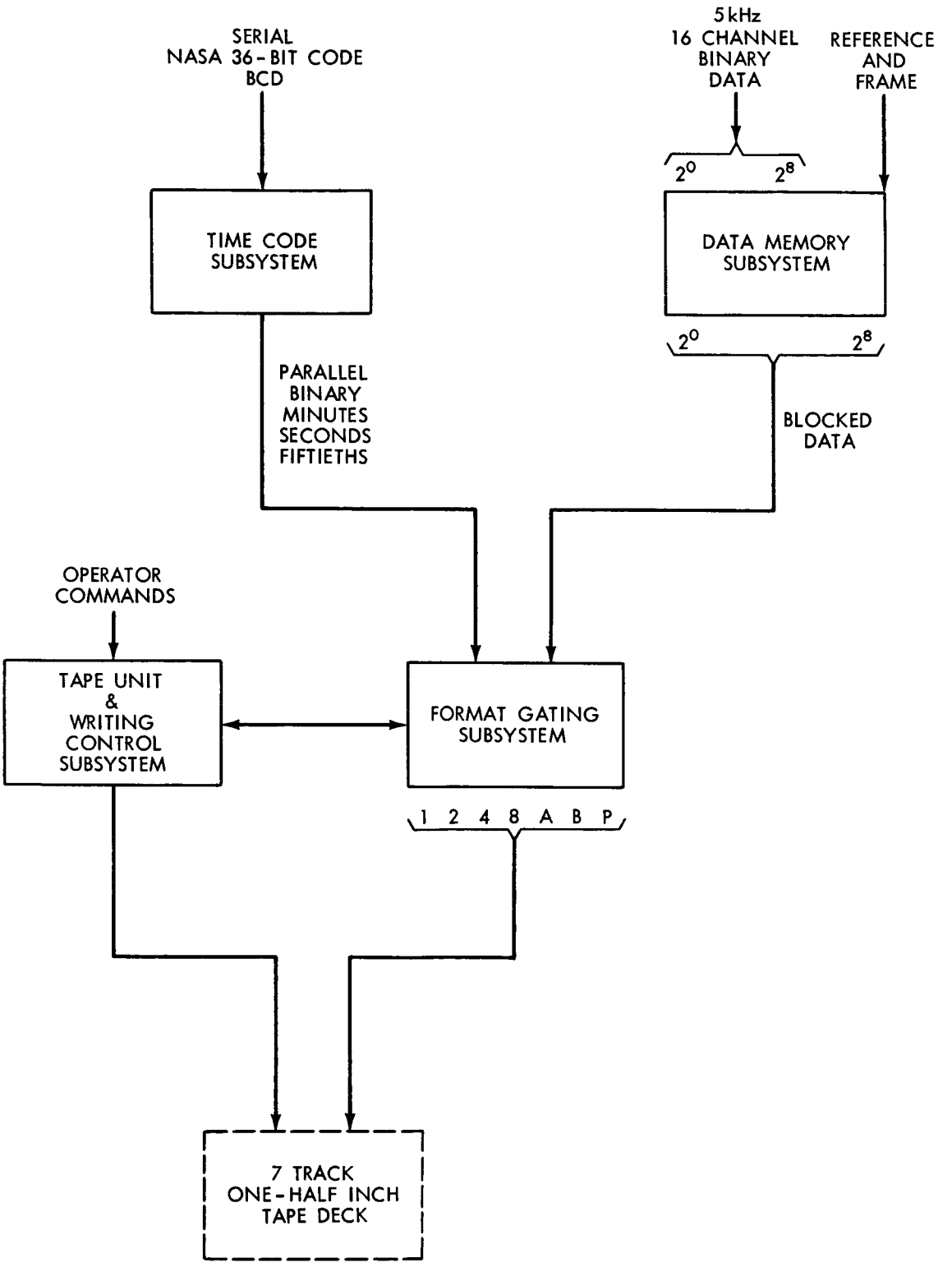


Figure 2. Data Format Converter Subsystems

The input of the time-code subsystem consists of serial binary-coded-decimal (BCD) time information in the NASA 36-bit format. This time code is generated during rocket flight (real flight or simulated) and recorded on tape. The time-code subsystem yields outputs of fiftieths of a second, seconds, and minutes in a parallel binary format. These outputs are transferred to the format-gating subsystem and then combined with data-bit outputs that are generated by the data-memory subsystem. Figure 3 illustrates the NASA 36-bit time code format.

Data input to the data-memory subsystem is a nine-bit parallel word occurring continuously at a 5-kilohertz rate. After 48 words are transferred to the data memory subsystem (3 data samples of each of 16 channels), they are transferred to the format gating subsystem at a 31-kilohertz rate. This procedure, in effect, converts the continuous data input into 48-word blocks. If the read-in time for 48 words is T, the output time is T/6. Thus, for 5T/6 the memory system has no output. So, during one-sixth of the time, data is transferred onto the 1/2-inch digital output tape, while for five-sixths of the time, the tape receives no data.

Sounding rocket data and time information are gated by the format-gating subsystem to provide the required format output. Counting-circuits provide proper synchronization for the format-gating subsystem. A seven-pin connector on the format-gating subsystem is the means of transferring data outputs to the magnetic tape.

Upon proper commands from the system operator, the tape unit and the writing-control subsystem provide signals for system operation and for the output-tape deck control.

Time Code Subsystem

The time code subsystem accepts the NASA 36-bit unmodulated time code from any source having an output equivalent to that of the Hyperion time-code generator. As an option, a time code at one-half or one-quarter speed can be used by proper selection of format speed. One-half speed corresponds to a 10-kilohertz data sampling rate, and one-quarter speed corresponds to a 20-kilohertz data sampling rate. It is necessary to detect the beginning of the 36-bit time code to provide a synchronization pulse for the time-code circuits. This is done by using Cards 2A and 9. The resultant output marks the beginning of a new 36-bit word.

Minutes, seconds, and fiftieths of a second time information are printed, eventually, on the output tape record. Each number can be represented by six

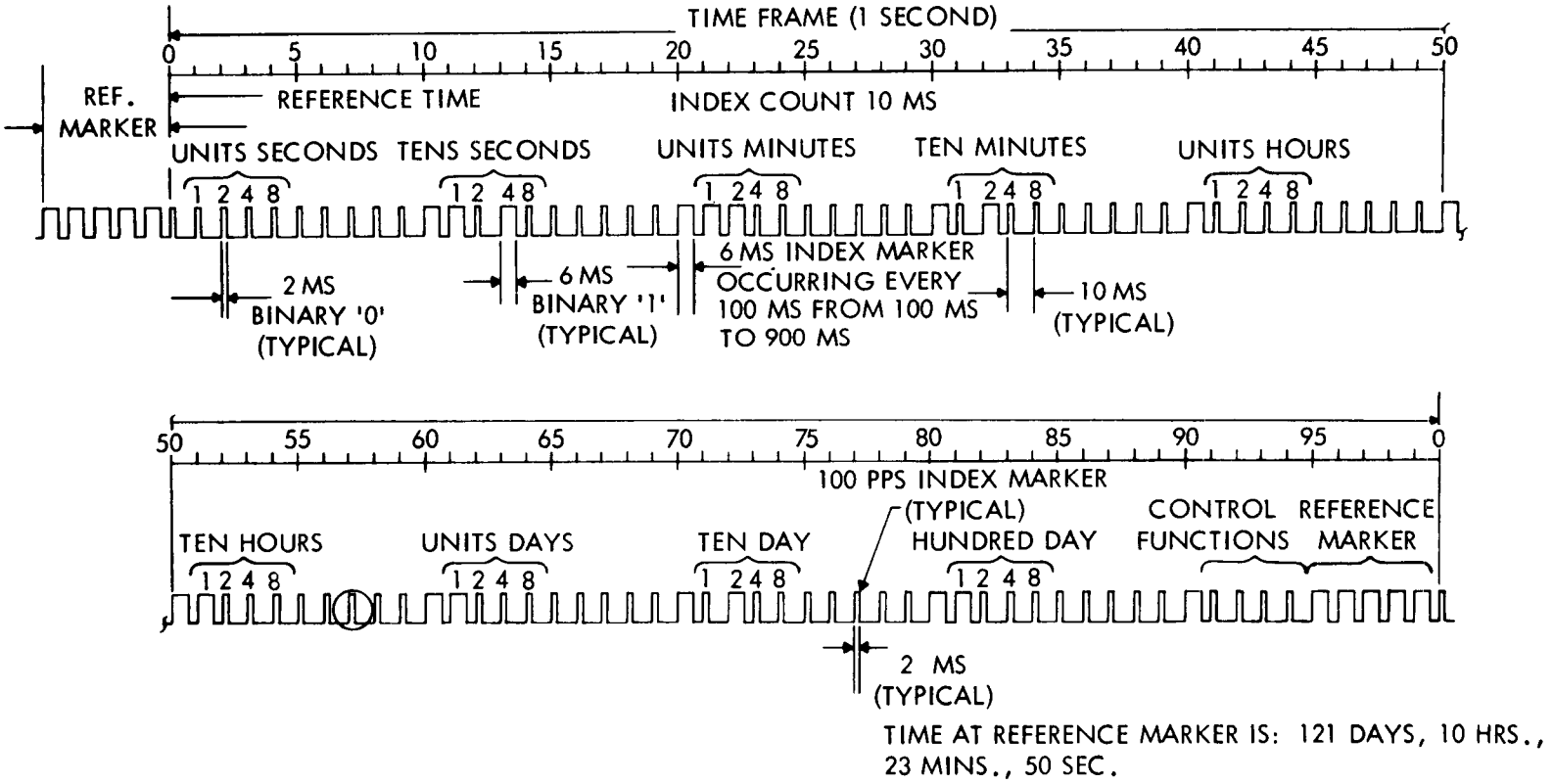


Figure 3. NASA 36-Bit Time Code Format

binary bits (2^0 through 2^5). See Figure 4 for the placement of these 6-bit characters.

Logic Cards 3, 4, 5, 6, 7, and 9 show the functional operation of the time code subsystem. The time code enters Card 3 in a BCD serial format for level conversion. Cards 4 and 5 convert the serial BCD to parallel binary form; Card 5 converts minutes and seconds only. Seconds information is held and gated by Card 7. Minutes information is held and gated by Card 6. The greatest time resolution, in fiftieths of a second, is provided by binary counting of the 36-bit time code. There are 100 pulses per second; these are divided by 2, prior to being counted. The resultant information is held and gated as needed by Card 9.

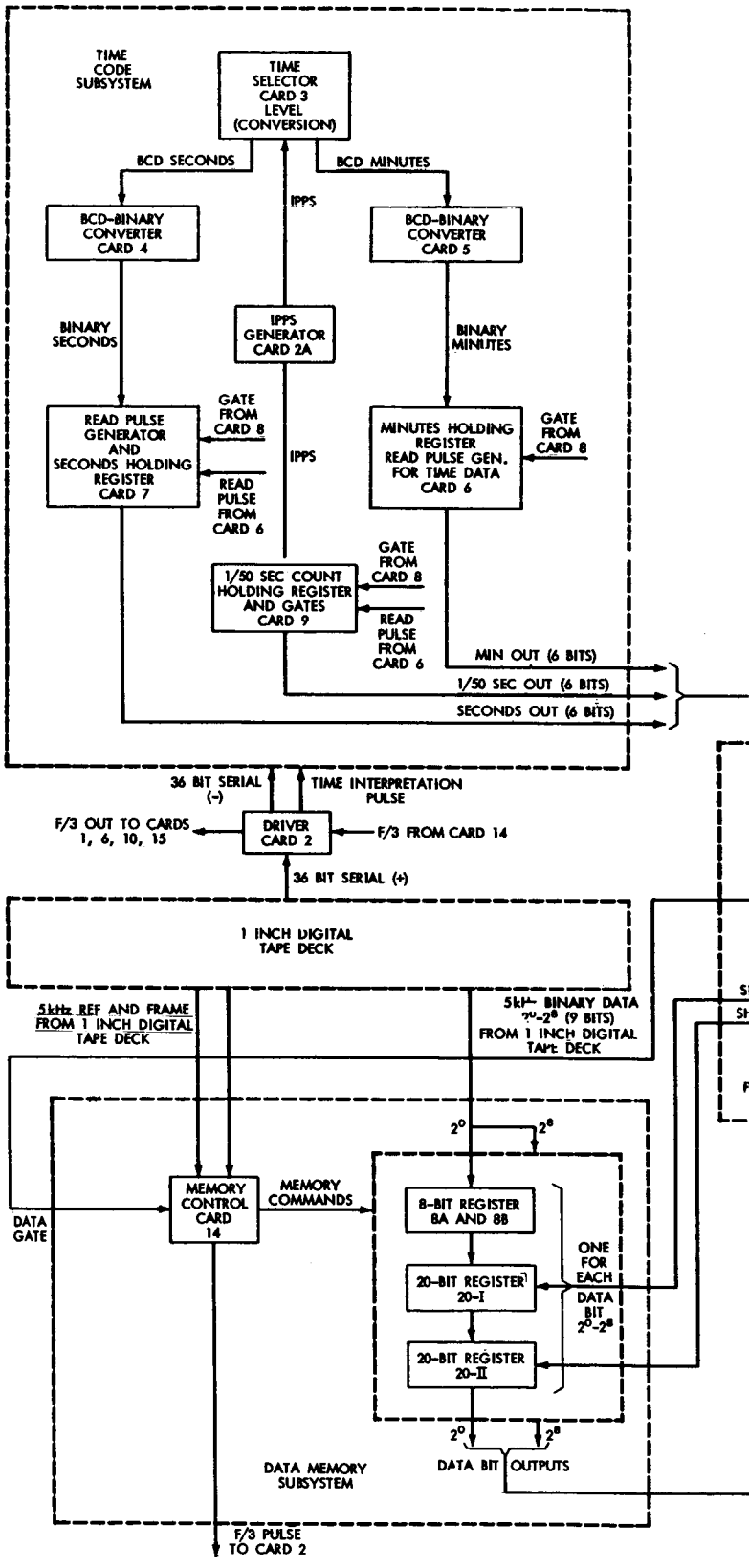
Data Memory Subsystem

The basic function of the data format converter is to take 9-bit, parallel, 5-kilohertz PPM telemetry data and provide a blocked binary tape suitable for computer use. The data memory subsystem accomplishes the blocking of data as follows:

The binary data information input to the Data Format Converter consists of parallel binary bits 2^0 through 2^8, at a 5-kilohertz rate. To provide spacing between records, the final output tape is blank five sixths of the time. Since the input data flows at a continuous rate, a memory system is needed to accept data at the input rate of 5 kilohertz, and also to provide a data output at the high rate of 31 kilohertz. Three frames of data; that is, 48 binary readings (bits 2^0 to 2^8) are stored in a shift register at the reference pulse rate of 5 kilohertz. Once stored, the 48 readings are shifted out, at the rate of 31 kilohertz, to the format gating subsystem. The shift-out time is less than one sixth of the shift-in time, therefore, during five sixths of the time there is no data output.

The memory system for each data bit (there are a total of nine) is composed of four sections: 8-bit register 8A, 8-bit register 8B, 20-bit register 20-I, and 20-bit register 20-II. (See Figures 5 and 6.)

As an example of subsystem operation, suppose 8A, 20-I, and 20-II bit registers are filling with 48 data bits at a rate of 5 kilohertz. Once filled, these registers are emptied at the clock-out rate of 31 kilohertz, while register 8B accepts the input data at 5 kilohertz. During the time 8B register becomes filled, 20-I becomes empty; 8B then connects to 20-I and both continue to fill at 5 kilohertz. About 1 millisecond later, 20-II register becomes empty then connects to 20-I. The three registers fill until 48 bits are stored, then shift out to the format gating subsystem, at the rate of 31 kilohertz. Memory control card 14 directs memory operation. The memory subsystem is controlled by the counting and gating circuits of the format gating subsystem.


TIME CODE SUBSYSTEM
TIME SELECTOR CARD 3 LEVEL (CONVERSION)
BCD SECONDS
BCD MINUTES
IPPS
BCD-BINARY CONVERTER CARD 4
BCD-BINARY CONVERTER CARD 5
BINARY SECONDS
IPPS GENERATOR CARD 2A
BINARY MINUTES
READ PULSE GENERATOR AND SECONDS HOLDING REGISTER CARD 7
GATE FROM CARD 8
READ PULSE FROM CARD 6
IPPS
MINUTES HOLDING REGISTER READ PULSE GEN. FOR TIME DATA CARD 6
GATE FROM CARD 8
1/50 SEC COUNT HOLDING REGISTER AND GATES CARD 9
GATE FROM CARD 8
READ PULSE FROM CARD 6
MIN OUT (6 BITS)
1/50 SEC OUT (6 BITS)
SECONDS OUT (6 BITS)
36 BIT SERIAL (-)
TIME INTERPRETATION PULSE
F/3 OUT TO CARDS 1, 6, 10, 15
DRIVER CARD 2
F/3 FROM CARD 14
36 BIT SERIAL (+)
1 INCH DIGITAL TAPE DECK
5kHz REF AND FRAME FROM 1 INCH DIGITAL TAPE DECK
5kHz BINARY DATA 2⁰-2⁸ (9 BITS) FROM 1 INCH DIGITAL TAPE DECK
2⁰
2⁸
MEMORY CONTROL CARD 14
MEMORY COMMANDS
DATA GATE
8-BIT REGISTER 8A AND 8B
20-BIT REGISTER 20-I
20-BIT REGISTER 20-II
ONE FOR EACH DATA BIT 2⁰-2⁸
DATA MEMORY SUBSYSTEM
DATA BIT OUTPUTS
F/3 PULSE TO CARD 2

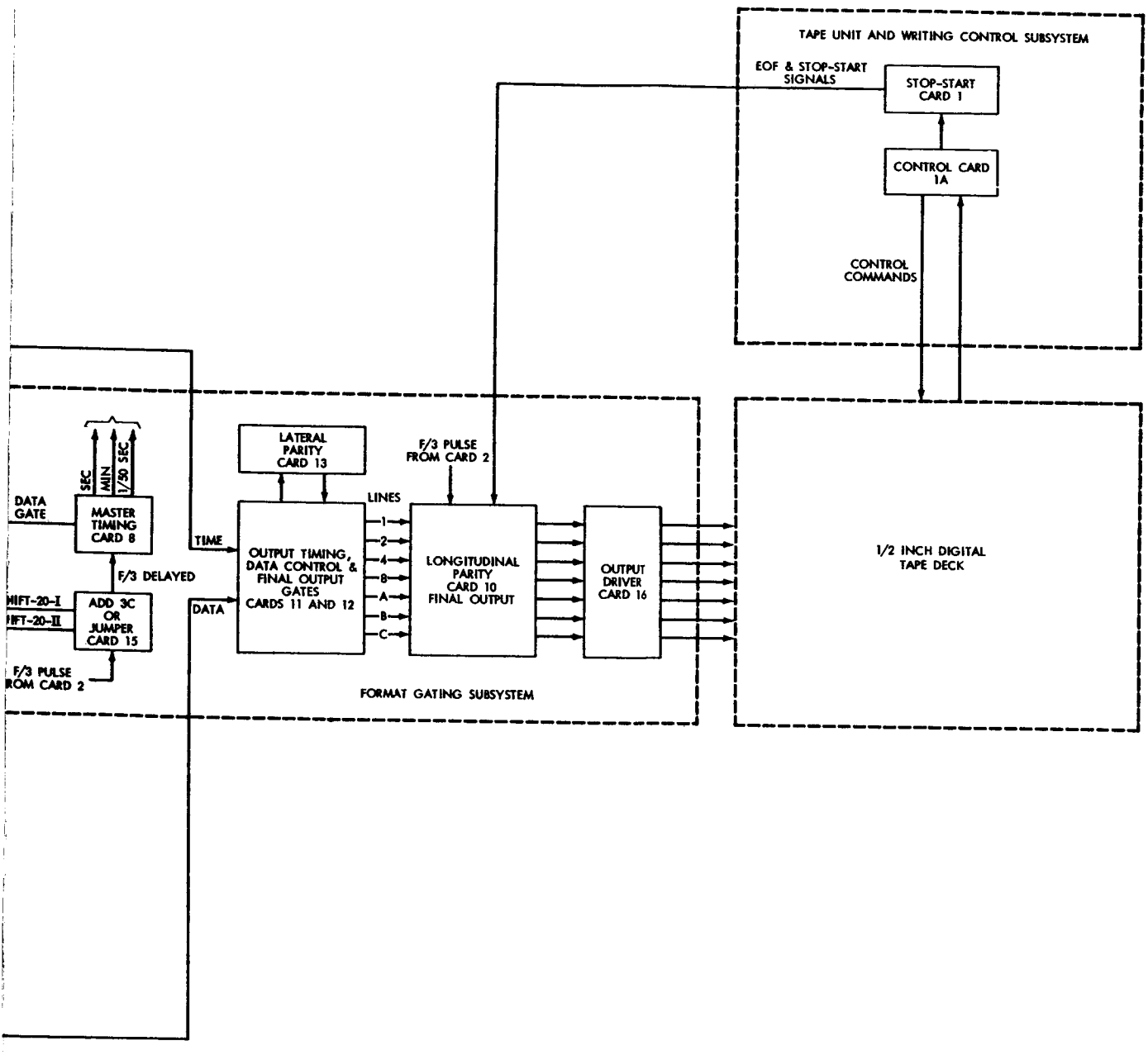


Figure 4. Data Format Converter, Functional Block Diagram

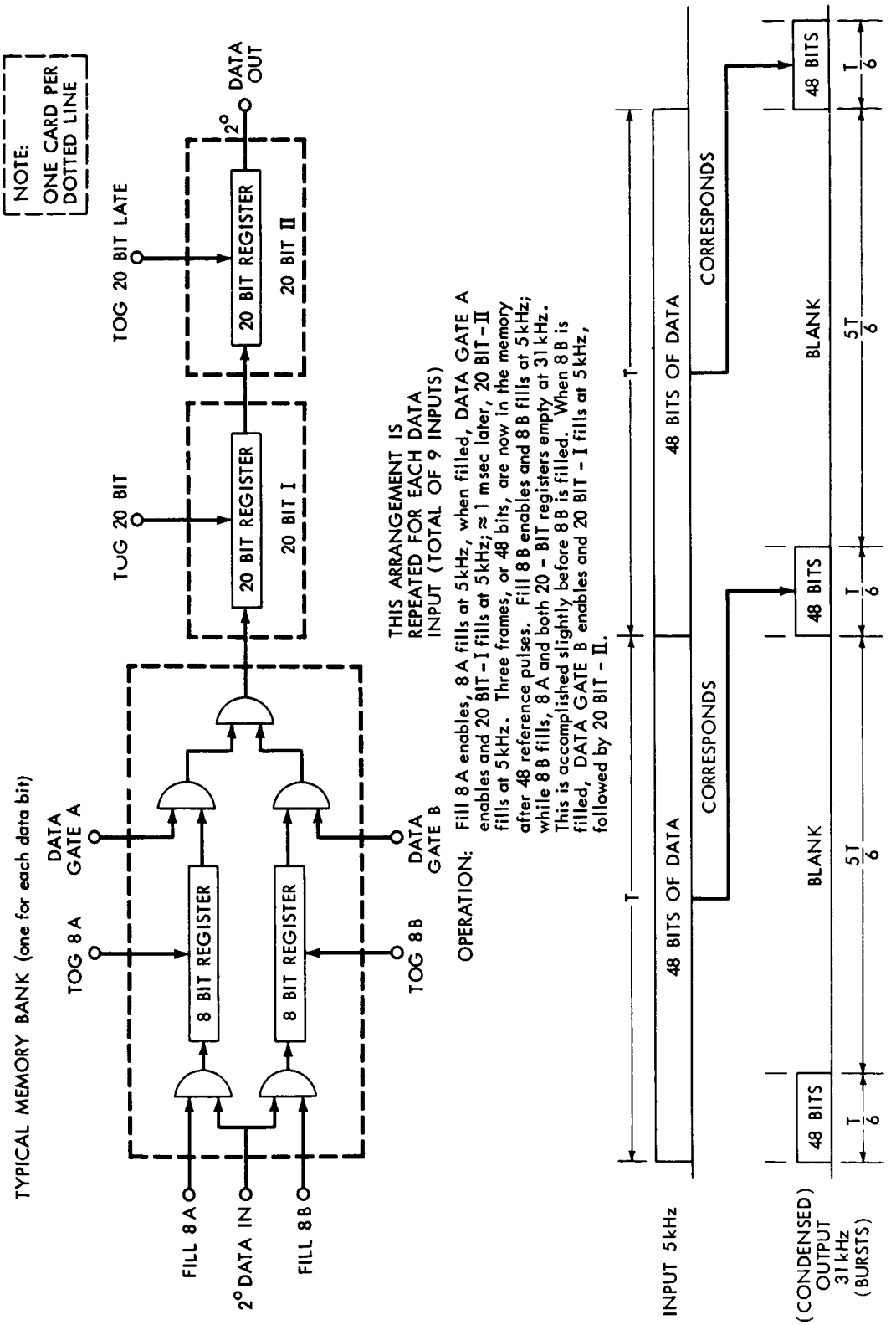
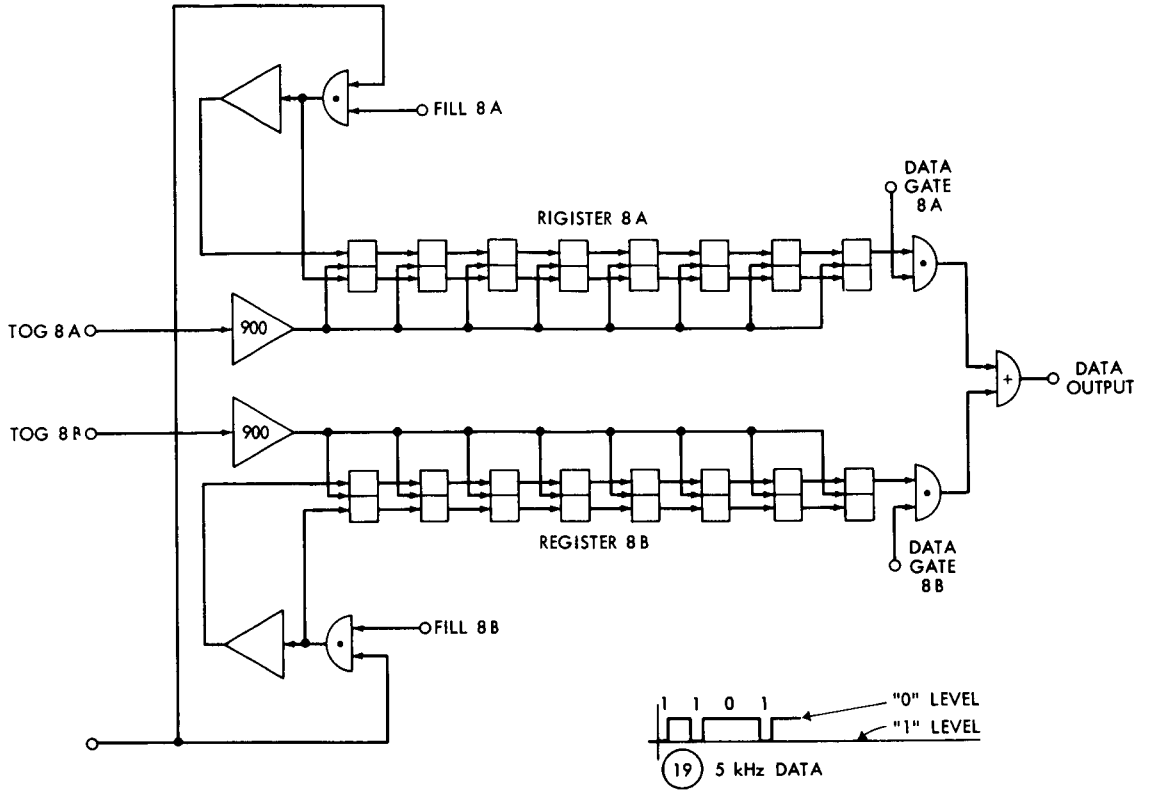


Figure 5. Operation of Memory Subsystem



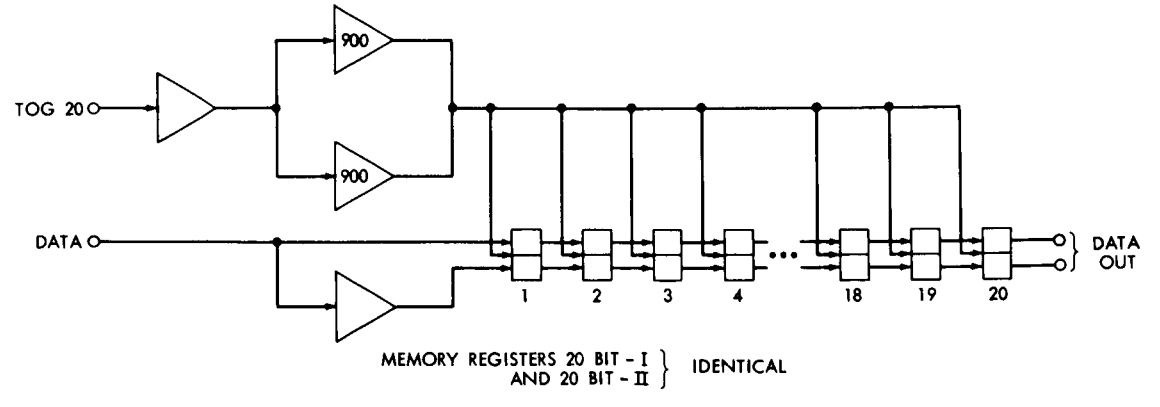


Figure 6. Operation of Memory Subsystem Registers

Format Gating Subsystem

The format gating subsystem provides gating and timing functions for the Data Format Converter. This subsystem is comprised of the following circuit cards. Master timing card 8 provides almost all of the timing signals for the Data Format Converter. Two cards, 11 and 12, provide gating for the final 7-channel output (six channels for data and time, plus one for lateral parity). As shown in the record format (Figure 7), several kinds of information may appear on any one channel. The final output gates select the correct information for any one channel, and also select the correct information to fill a particular character. All gating circuits are so arranged that a particular function is not changing while it is being gated to the output.

Card 15 modifies the outputs from Card 8 so that an optional record format can be selected. If Card 15 is not used (the original 99 character record selected), Card 15 Jumper must be substituted.

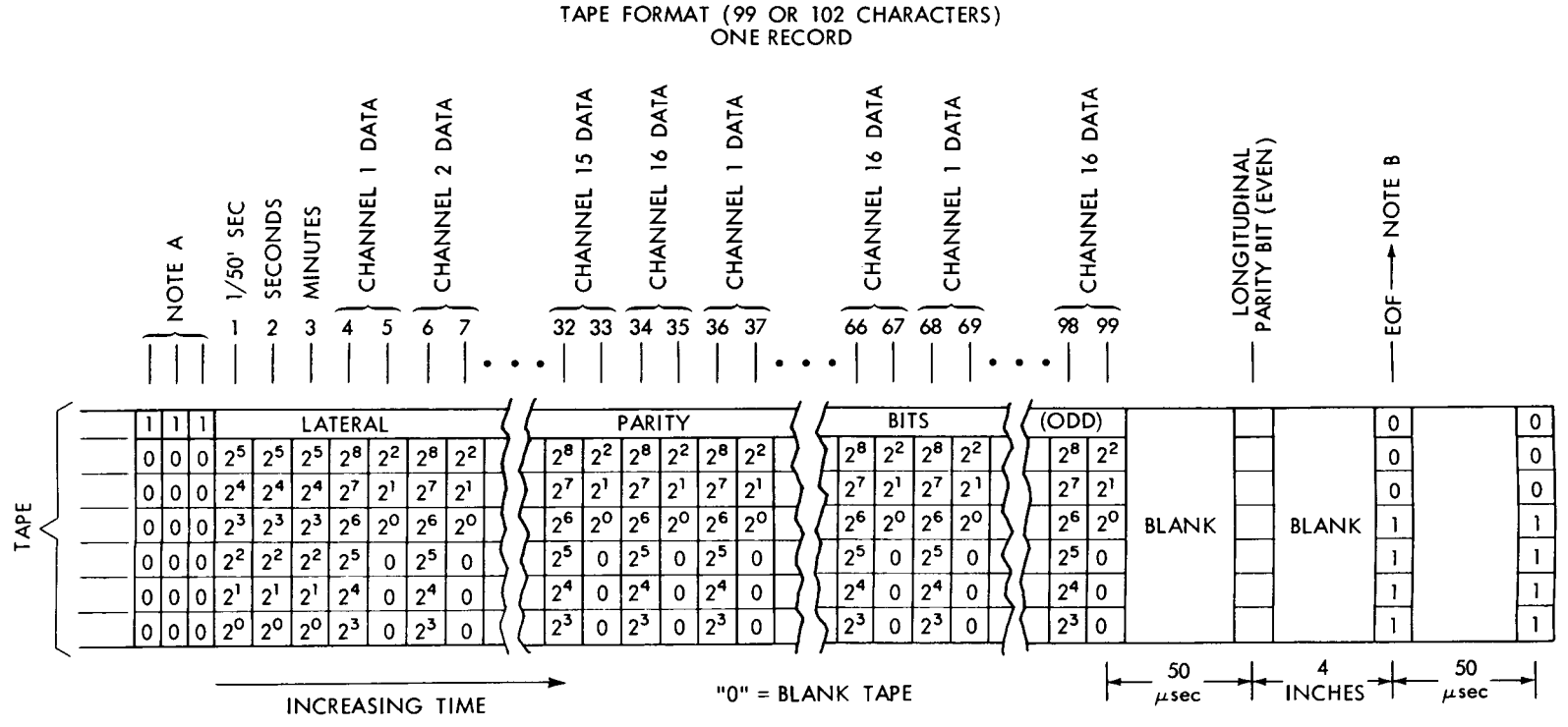
Lateral and longitudinal parity circuits are also provided for the required tape checks. Card 10 generates longitudinal parity character and EOF marker and check character. Output driver card 16 provides a seven channel output to the CEC magnetic tape.

TAPE FORMAT

The tape format produced by the Data Format Converter was so designed that the size of the memory system would be minimal. Data enters the system at a 5-kilohertz rate, but is written on the tape at a 62-kilohertz rate. Data are stored before written, and the more data in a record, the more storage required. For this reason, only three frames of data (three readings of sixteen channels) are in an output record.

On the 99-character record, (Figure 7) the first three characters contain time; the next two characters contain the first reading of channel one. There are, all together, 48 readings of data in 96 characters since each reading requires two characters. (Note that the second character of a particular reading is not full. This allows for an increased number of bits in a data reading.)

In the optional 102-character record, three blank characters are added to the front of the 99-character format. These characters contain only parity bits. All records are followed by a longitudinal parity character. Parity is an even number of bits. The check bit of the lateral parity line is determined by the



NOTE A: The optional card 15 will add three extra characters, marked only by parity bits, for a total of 102 characters

NOTE B: The end of file marker is generated only when Data Format Converter is turned off. It is followed by a check character

The time code is printed first, followed by data and then the longitudinal parity character. There is a blank space of greater than 3/4 inch between records

Tape speed is 112.5 ips - 556 characters/inch - 62 kHz character rate

Figure 7. Tape Format

longitudinal circuitry. Therefore, the longitudinal check character can contain an even number of bits.*

When the Data Format Converter stops writing, the last record is completed and followed by an end-of-file (EOF) character, bits one, two, four, and eight. The end-of-file (EOF) character is also followed by a longitudinal check character, which is identical to the EOF character. Figure 7 shows the timing for the record format.

Tape Unit and Writing Control Subsystem

Stop-Start Card 1, Control Card 1A, and Driver Card 2 are the functional operation electronic circuits of the tape unit and writing control subsystem.

Card 1 controls the writing operation of the Data Format Converter. In the non-write condition, Card 1 disables the output circuits on the longitudinal parity card. When the WRITE command is given, circuitry on Card 1 completes the first record on the tape, not just a part of a record. When the WRITE command is removed (if a record is being written), the record is completed before writing stops. Precise timing circuitry provides an end-of-file marker.

Card 1-A provides signals for remote-control operation of the tape deck by the front-panel selector switch. Card 2 provides a 62-kilohertz signal and timing for 36-bit recognition at all frequencies.

CARD DESCRIPTIONS

Stop-Start Card (Card 1)

Card 1 starts and stops the output records of the Data Format Converter at the beginning and end of complete data records. See Figures 8 and 9 for the logic diagram and waveforms of card 1.

Normal Operation Mode

The normal operation mode is as follows: When the record switch is in the OFF position, the normally high (NH) output at pin terminal (26)** is zero volt, the normally low (NL) output at pin terminal (25) is +3 volts. Thus, both ground

*This format is based on an IBM standard program.

**For each logic card described, pin terminal locations are indicated by a circled number, both in text and on each logic diagram. The nomenclature preceding each called-out pin terminal identifies the type of pulse referred to.

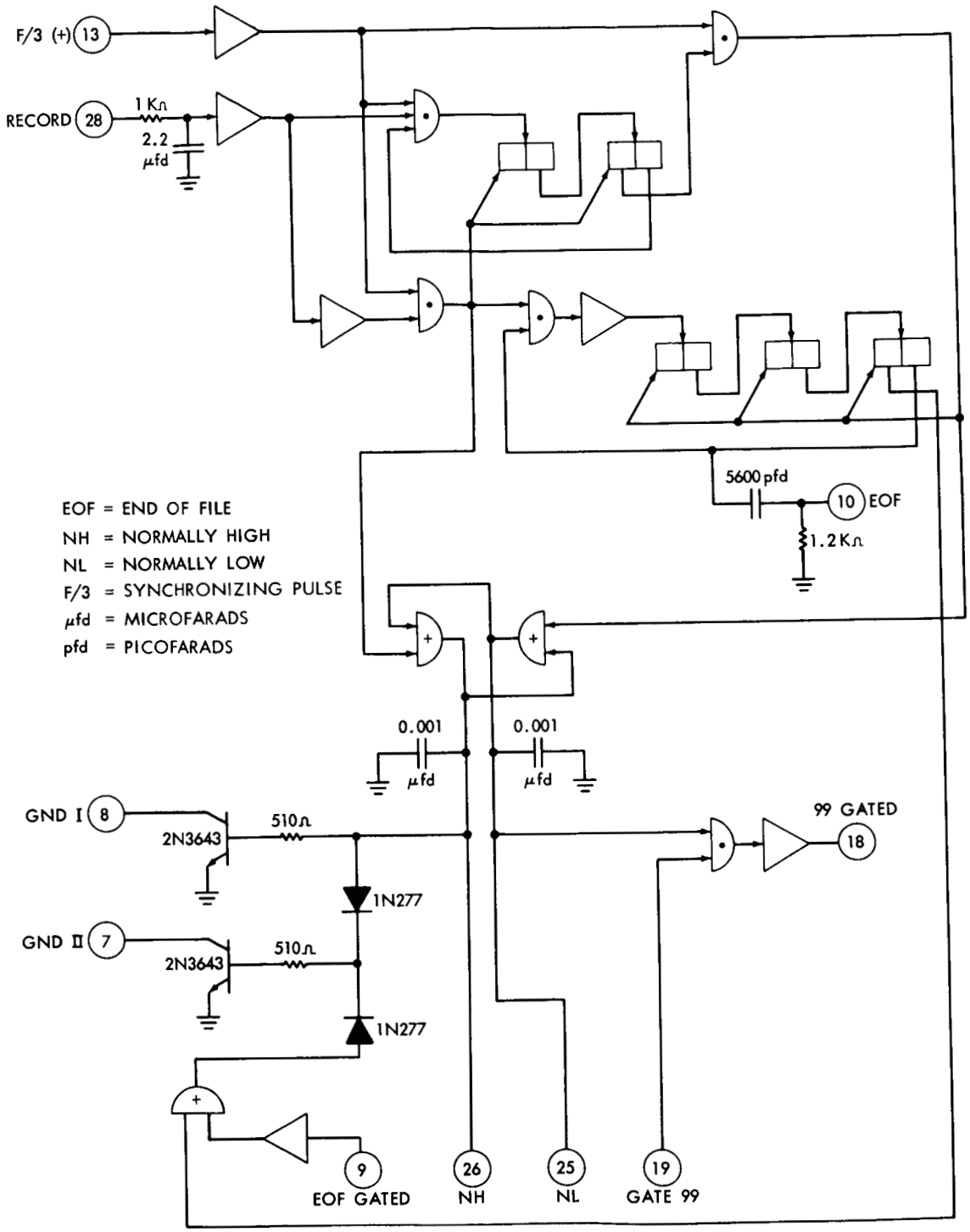


Figure 8. Stop - Start Card 1, Logic Diagram

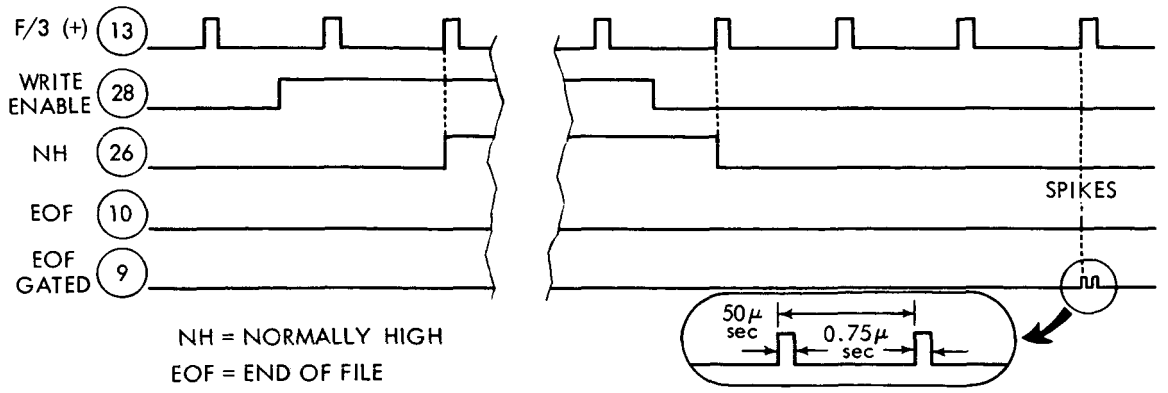


Figure 9. Stop - Start Card 1, Waveforms

transistors are open, and the 99 gated pulse at pin terminal (18) and the output timing pulse of card 11 are both inhibited.

Memory Control Card 14 provides the waveforms necessary for the operation of the Data Format Converter. Frame pulse at pin terminal (29) is reduced in repetition rate from 312 to 104 hertz. The F/3 output pulse at pin terminal (28) is the only output from Memory Control Card 14 which is necessary to check the operation of the Data Format Converter, without the remainder of the Data Memory Subsystem. When the switch is on the RECORD position, zero volt is applied to the 3 input AND gate, thus enabling it. Next, the F/3 pulses are counted, and on the second F/3 pulse, the state of binary A is reversed. NH output at pin terminal (26) goes to +3 volts and NL output at pin terminal (25) goes to zero volt. Both 2N3643 transistors are turned to ON, and the proper grounds are thereby provided to enable the operation of the 99 gated pulse and the output timing pulse of Card 11.

End-of-File Mark

When the record switch is turned to OFF, binary A is reset by the next F/3 pulse. Grounds I and II at pin terminals (8) and (9) are now removed, and the 99-gated and the output-timing pulses of Card 11 are again disabled. The F/3 pulses are counted to provide spacing for the end-of-file marker; the marker appears on the fourth F/3 pulse. The end-of-file marker fires the 0.75-microsecond one-shot multivibrator of the longitudinal parity card (Card 10), and, after a 50-microsecond delay, the 0.75-microsecond one-shot multivibrator fires again. Both 0.75-microsecond pulses are fed back into the Stop-Start Card (Card 1), to ground the OR gates of Ground II at pin terminal (7). The first end-of-file marker is thus printed twice, after which the Data Format Converter is turned to OFF. Using a 3M magnetic tape reader, the end-of-file mark can be seen about 4 inches after the last record on the tape.

Tape Deck Control Card (Card 1A)

When in the remote control mode, Card 1A provides command signals to the tape deck, and also provides a write-enable signal for the Data Format Converter. (See Figures 10 and 11.) Applying +3 volts to the inputs at pin terminals (6) and (7), (Figures 10 and 11) turns the Data Format Converter to ON and to OFF, respectively. In the manual mode, a pushbutton switch controls this action; in the automatic mode, a relay in the Hyperion tape search unit controls the action. The positive signal activates an input flip-flop that removes switch or relay chatter. A transition in either direction by the flip-flop fires an adjustable-delay one-shot multivibrator.

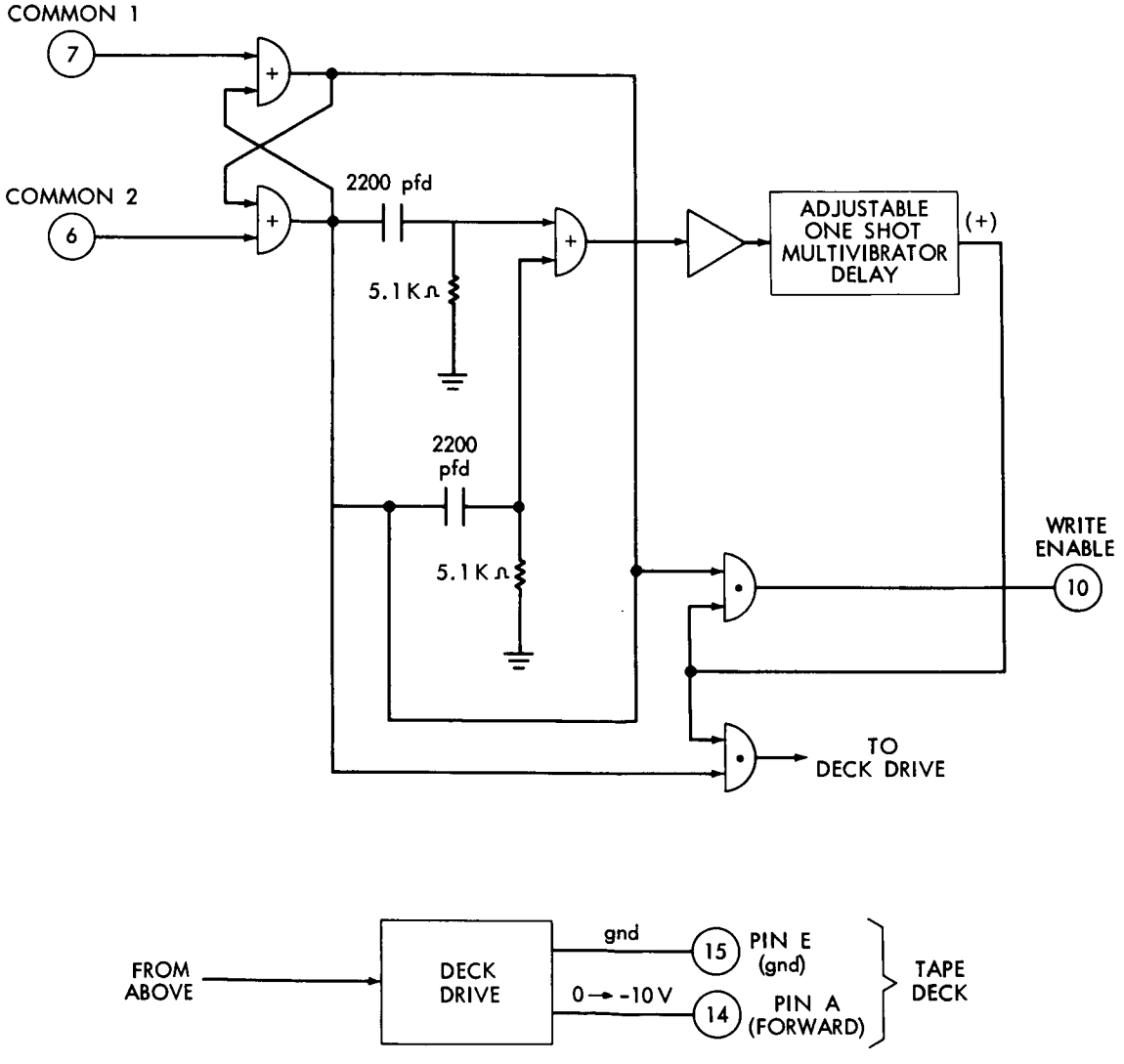


Figure 10. Tape Deck Control Card 1A, Logic Diagram

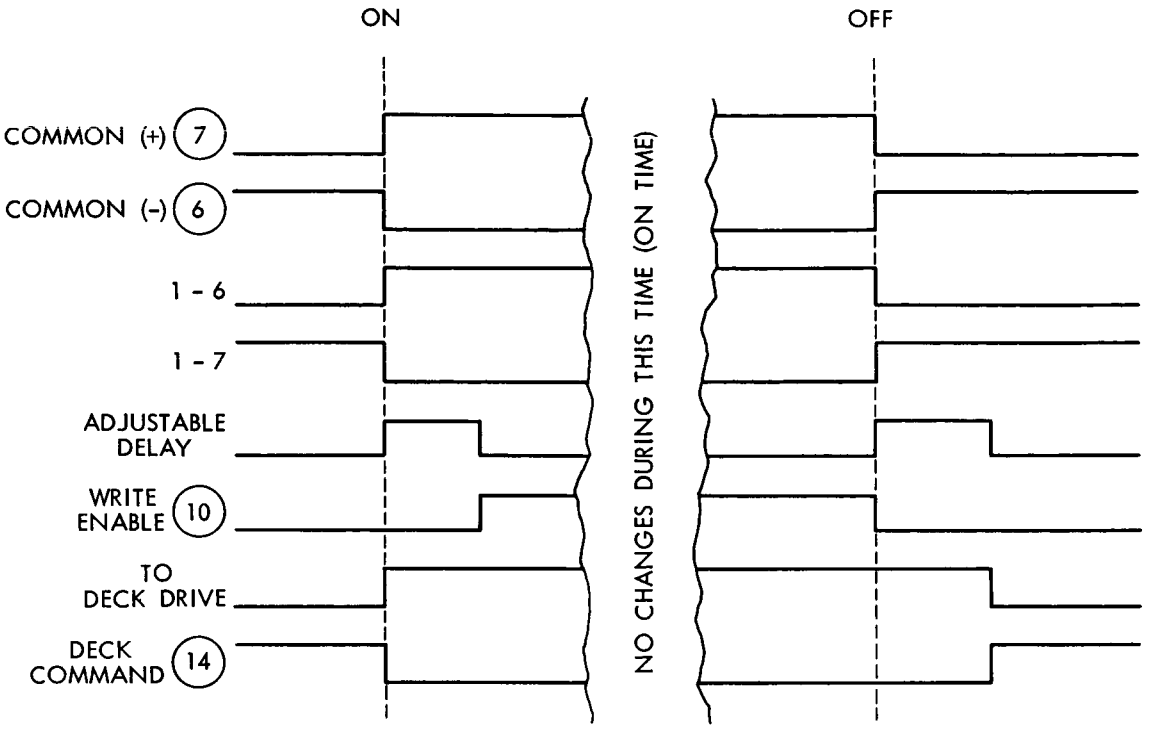


Figure 11. Tape Deck Control Card 1A, Waveforms

When the Data Format Converter is turned to ON, the forward command to the tape transport occurs immediately, and after the delay, the write-enable signal goes positive, enabling the Data Format Converter. When switched to OFF, the write-enable signal goes to zero volt immediately, and after the delay, the forward command to the tape transport is removed.

Driver Card (Card 2)

Card 2 provides many of the waveforms used in the Data Format Converter in addition to providing the 62-kilohertz clock pulse for the entire system. (See Figures 12 and 13.) The clock pulse is generated by a highly stable, adjustable, Clapp oscillator which drives a logic one-shot multivibrator with a 4-microsecond period. The output is a +3 to zero volt, 4-microsecond pulse, occurring at a 62-kilohertz rate.

Pulses for the interpretation of the 36-bit time code are also provided on this card. At the real time rate of 5 kilohertz, the 36-bit time code from the Hyperion time-code generator, or from the PI tape deck, is a pulse-width modulated binary signal. A logical 1 pulse is 6 milliseconds, and logical zero pulse is 2 milliseconds. For the time to be correctly interpreted, a 0.3-millisecond comparison pulse is created after a zero (but during a 1). (See Figure 13.)

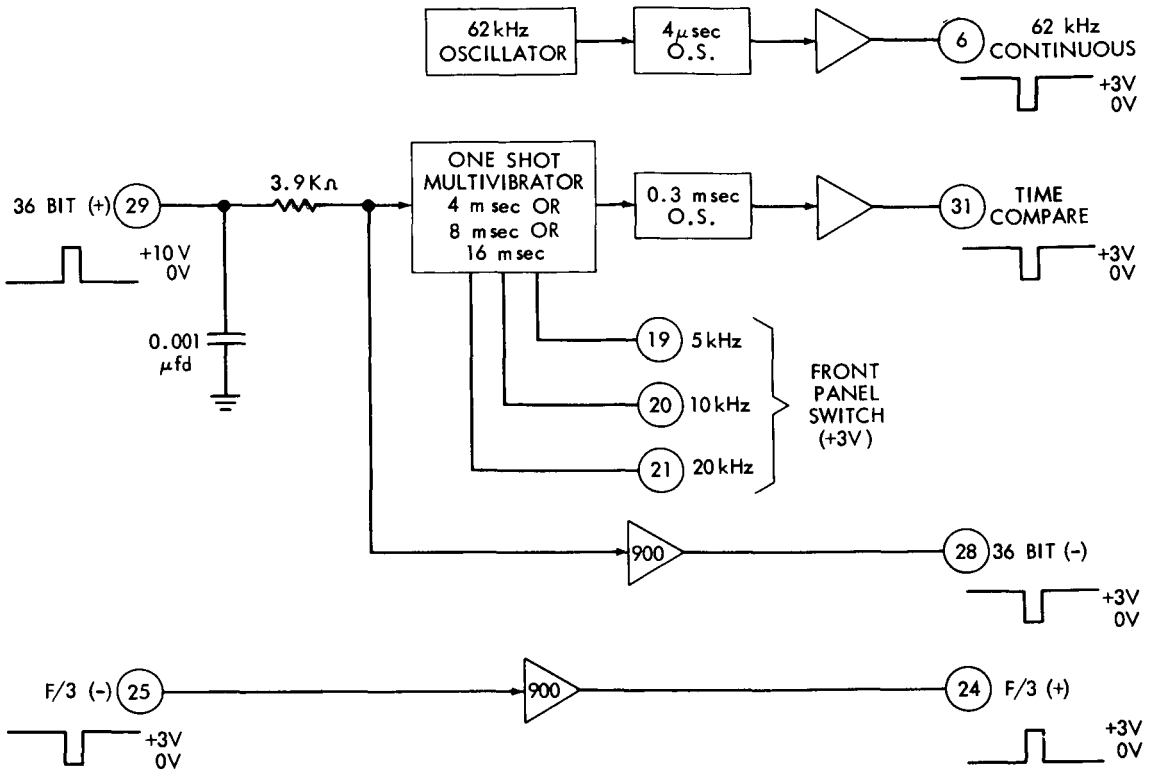


Figure 12. Driver Card 2, Logic Diagram

At one-half or one-fourth speed, the pulse changes to 8 and 16 milliseconds, respectively (Figure 12). Timing changes are made by changing resistors with a switch. The resultant pulse, the time compare at pin terminal (31), goes from +3 to zero volt. Also, the 36-bit time code is provided as a +3-to-zero-volt signal from a high fanout driver circuit. A high fanout driver circuit is provided on this card for the F/3 pulses. Its output, F/3 at pin terminal (24) is a positive going pulse, and is used throughout the Data Format Converter system.

1 PPS Generator Card (Card 2A)

Card 2A generates a one pulse per seond (1 PPS) pulse from the 36-bit time code. The pulse should last from the beginning of the T=0 marker until the beginning of the first bit, a total time of 10 microseconds. (See Figures 14 and 15.) The 1 PPS pulse is generated by simply resetting a JK flip-flop with the 1/50-second AND gate, which occurs at exactly T=0, and then setting the flip-flop again with the leading edge of the first bit of the 36-bit time code [36 bit (-)] at pin terminal (28).

When the system is first turned on, however, the 1/50-second counter starts counting in the middle of the time code. It is therefore necessary to reset the

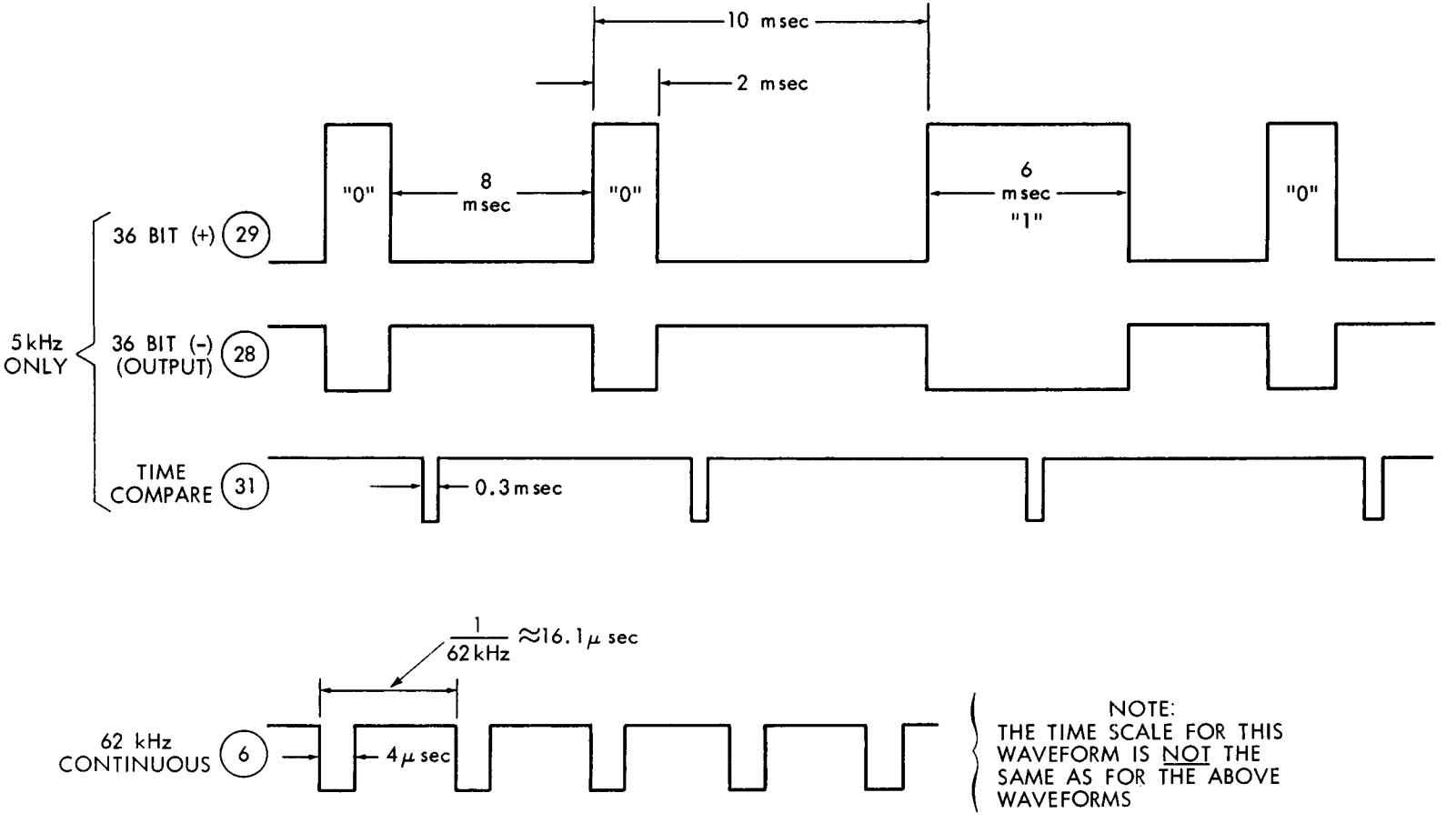


Figure 13. Driver Card 2, Waveforms

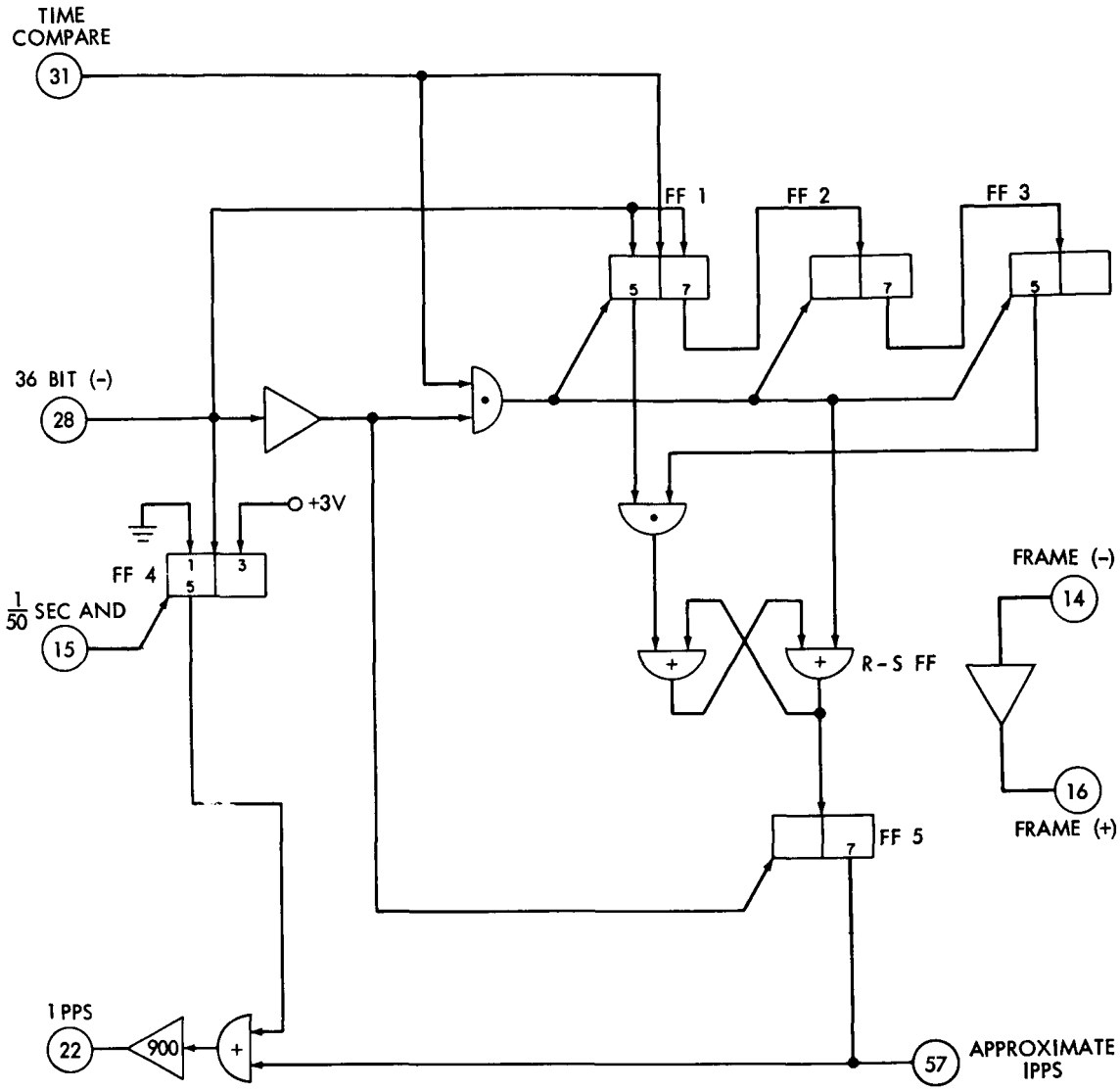
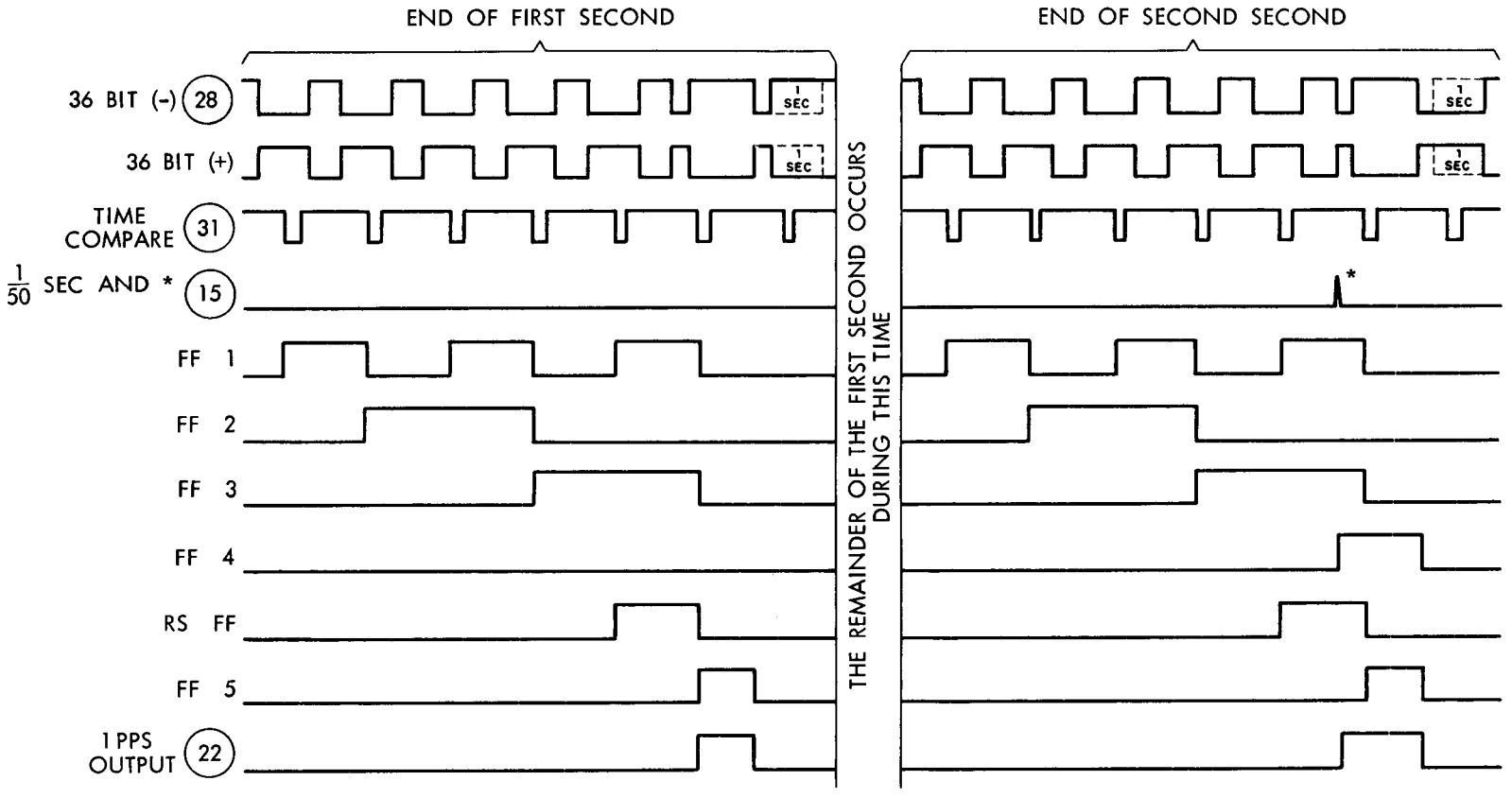


Figure 14. 1 PPS Generator Card 2A, Logic Diagram

1/50 second counter to zero at the proper time. Since this is normally done with the 1 PPS pulse (which, in turn, depends on the 1/50-second AND gate), it now becomes necessary, for original system synchronization, to provide an approximate 1 PPS pulse which does not depend on the 1/50-second counter. This can be done by counting ones of the 36-bit time code, to establish a recognition pattern of the time when five ones are followed by a zero. This condition can occur only during the time period prior to T = zero. The 1 PPS pulse generated by this recognition pattern is approximate, because the recognition



* The $\frac{1}{50}$ SEC AND is only nanoseconds long when the circuit is working properly and it therefore cannot be seen on a scope.

Figure 15. 1 PPS Generator Card 2A, Waveforms

pattern is not complete until after the start of the 1 PPS pulse, and the pattern is required to produce synchronization for the 1/50 second counter. The 1/50 second counter then counts to fifty, which occurs exactly at T=zero. This signal is OR gated with the approximate 1 PPS pulse, thus producing the desired 1 PPS pulse which begins a T=zero and lasts 18 milliseconds.

Time Selector Card (Card 3)

Card 3 selects the required time information from the incoming 36-bit word, and also supplies to the BCD-to-binary converters (cards 4 and 5) the read and gate pulses necessary for the BCD-to-binary conversion. See Figures 16 and 17.

Of the time information available in the 36-bit code, only seconds and minutes information is used; that is, only the first four bits of the first four 10-bit words are used. Referring to the block diagram and the waveforms, the 36-bit input at pin terminal (29), from driver Card 2, is inverted as shown. Flip-flops I, II, III, and IV count to 10, four times. Flip-flop IV is zero for four counts, and 1 for six counts. The output of flip-flop IV gates the desired information from the 36-bit code. Flip-flops A and B allow four counts of ten to occur, then stop the operation until they are reset by the 1 PPS pulse at pin terminal (21). In the resulting pulse train, the data time output at pin terminal (31) is high, except when a 1 appears on the time code as shown.

Read 1 output, at pin terminal (30), goes high at the end of the allotted time for 1 in the 36-bit code. Read 2 output, at pin terminal (26), goes high at the end of the time allotted for 2 in the time code. Read 4 output, at pin terminal (22) and read 18 output at pin terminal (18), operate in a similar manner.

The gate outputs for 1, 2, 4, and 8 seconds, at pin terminal (15), is low only during the intervals indicated. The other gate outputs, at pin terminals (6), (10), and (14), are similar. The time reset output, at pin terminal (20), is a positive-going pulse at the end of the 1 PPS pulse at pin terminal (21).

BCD-Binary Converter Cards (Cards 4 and 5)

Decimal digits are usually coded in binary numbers, and physically implemented by binary-state devices. A binary-coded decimal (BCD) number system is thus one in which the decimal digits are represented by a binary code.

When properly interconnected with time selector Card 3, the BCD-binary card converts the BCD code of the 36-bit Hyperion format to a binary representation (Figure 18). Card 4 converts seconds, and Card 5 converts minutes. The conversion is accomplished in a serial manner, from the serial BCD input, with

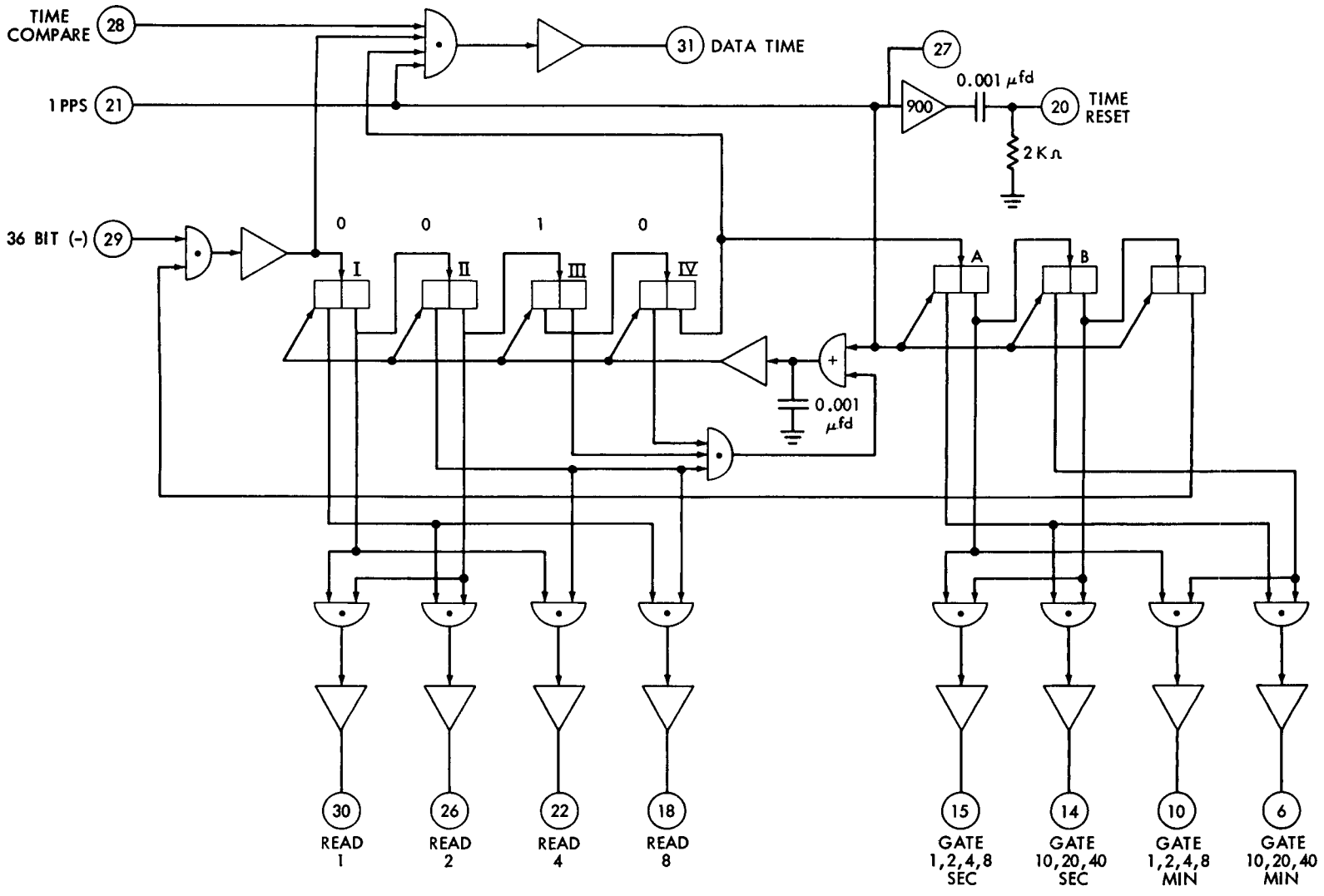


Figure 16. Time Selector Card 3, Logic Diagram

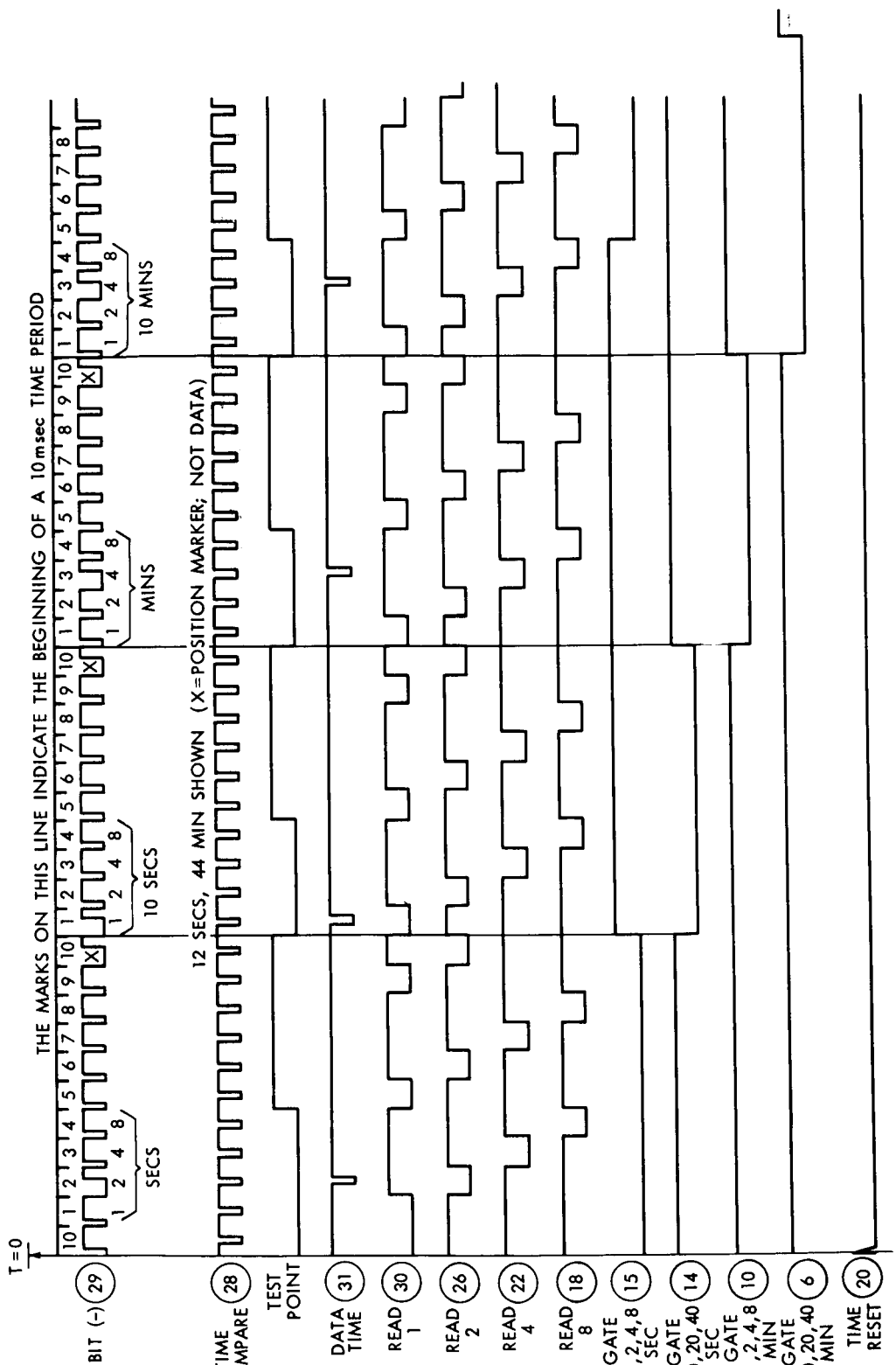


Figure 17. Time Selector Card 3, Waveforms

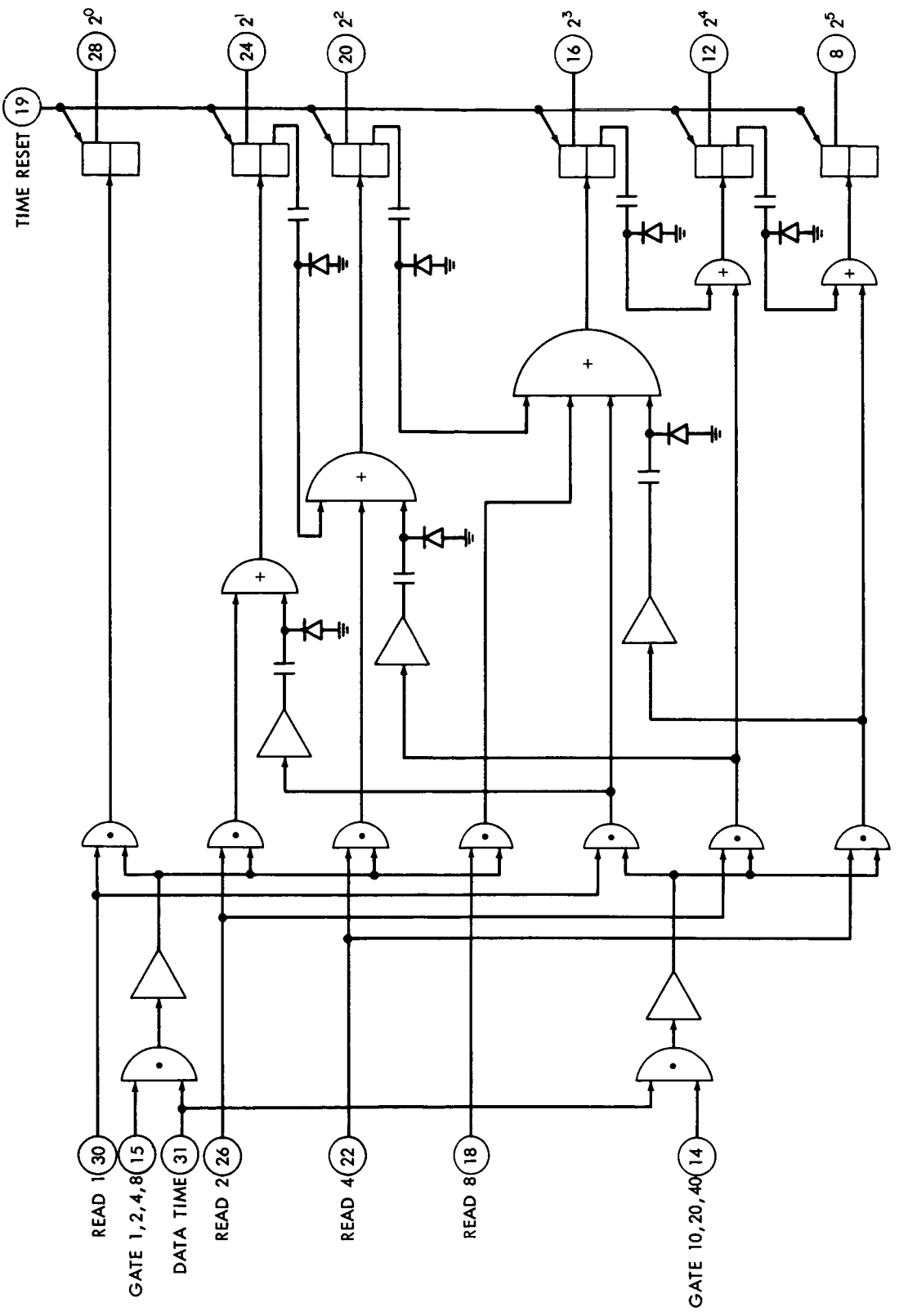


Figure 18. BCD – Binary Converter Cards 4 & 5, Logic Diagram

the final result held in flip-flops 2^0 through 2^5, as shown in Figure 18. The flip-flops are read at the next 1 PPS pulse, so that the time read is always 1 second late; that is, the time read refers to the preceding second.

General circuit operation is as follows; suppose reset at pin terminal (14) has occurred, it resets all output binaries to zero. This reset also occurs at the end of the 1 PPS pulse. One of the unit seconds appears as data time input at pin terminal (31), and its value (0 or 1) is transferred to the binary output 2^0 at pin terminal (28). Two is transferred to the binary output 2^1, at pin terminal (24), by the read 2 input at pin terminal (26). Digit four of the unit-seconds appears, and is transferred to 2^2 output at pin terminal (20).

Note that units of a BCD code (0 through 9) are the same as binary units. Ten is gated by 10, 20, 40 input at pin terminal (14) and transferred to 2^3 and 2^1. If 2^1 is 1, a carry digit to 2^2 occurs. This will be the case, with an input of 12. Twenty is transferred to 2^2 and 2^4. If 2^2 is 1, a carry occurs (as in 24) to 2^3. If 2^3 is 1, a carry to 2^4 occurs. Table 1 shows how some transfers from BCD to binary (including carry digits) occur in the numbers 1 through 59. Testing of the circuit should be done with the Hyperion time-code generator, in the preset mode of operation. The output number can then be advanced manually.

Read Pulse Generator, and Minutes and Seconds Holding Registers (Cards 6 and 7)

The read pulse generator produces pulses for the reading of the time-holding registers. The lack of synchronization between time and data signals necessitates this circuit. See Figures 19 and 20.

The seconds and minutes BCD-to-binary converter cards may be examined at any time during the 10-millisecond 1 PPS pulse at pin terminal (27) of Card 6. Flip-flop A is set by the 1 PPS pulse. The minute and seconds will not change for 10 milliseconds. One F (+) pulse at pin terminal (28) of Card 6 will reset flip-flop A during this 10 milliseconds, since the frequency of the F/3 pulse is 104 hertz and 1/104 less than 10 milliseconds. This procedure ensures that the minutes-and-seconds holding-registers are updated each second. Flip-flop B is set at the same time as is the edge of the pulse which causes the 1/50-second count to be updated by one. It will remain set for 0.1 microsecond to allow the counting to occur and will then be reset by the F/3 pulse. Resetting produces the read signal for the 1/50-second holding register. In the final output, the same 1/50 second will generally appear three times, since the frequency of the F/3 pulse is approximately greater than 3/50 second.

In summary, the minutes-and-seconds holding-registers are updated once each second, and the 1/50-second register is updated once each 1/50 second.

Table 1
Data Format Converter
BCD - Binary Converter Cards
Card 4 and Card 5

The following table shows how representative numbers 10, 16, and 59 enter in BCD and how they are transferred to binary output flip-flops 2^0 through 2^5. Essential to the conversion process is the carry operation performed whenever a particular flip-flop counts twice. The least significant BCD bits are received first.

NUMBER	BCD INPUT							BINARY OUTPUT					
	1	2	4	8	10	20	40	32	16	8	4	2	1
10					1			FINAL ANSWER 0	0	1	0	1	0
16		1										1	
			1								1		
					1					1		1	
								CARRY	1	1	1		
								FINAL ANSWER 0	1	0	0	0	0
59	1												1
				1						1			
					1					1		1	
							1		1		1		
								CARRY	1				
								FINAL ANSWER 1	1	1	0	1	1

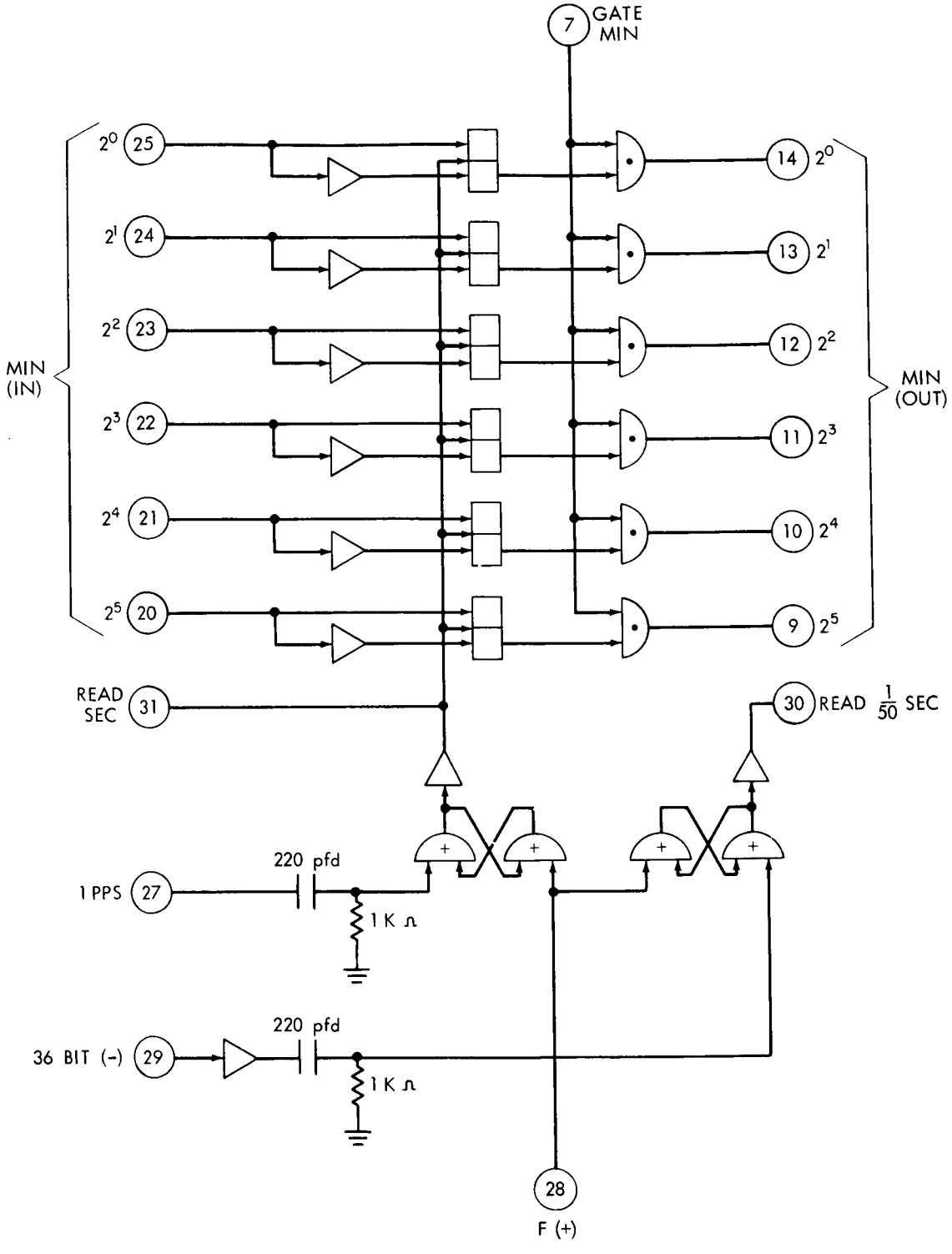


Figure 19. Read Pulse Generator and Minutes Holding Registery Card 6, Logic Diagram

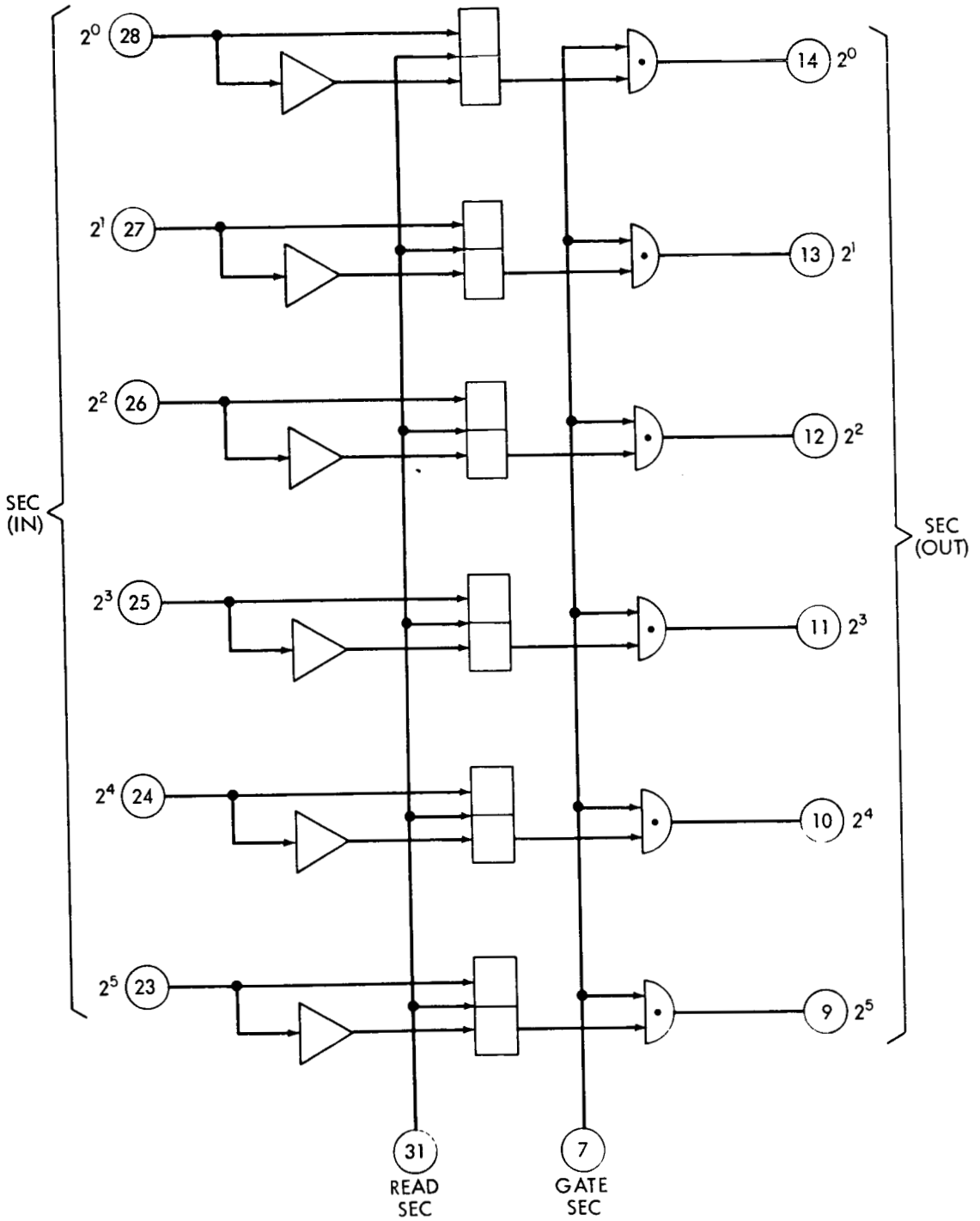


Figure 20. Seconds Holding Register Card 7, Logic Diagram

If any of the time information happens to be changing when an F/3 pulse occurs, no updating occurs. It will, however, be updated on the next F/3 pulse, 9 milliseconds later. This system ensures that the most recent possible time is always available to be read.

Master Timing Card (Card 8)

Card 8 provides the primary gating signals for the entire Data Format Converter. See Figures 21 and 22. The timing sequence begins with every F/3 pulse, at pin terminal (30). A 62-kilohertz oscillator, not in synchronization with the 5-kilohertz or frame pulses, provides pulses which are counted by flip-flops. After the F/3 pulse, ninety-nine 3-microsecond pulses are allowed to pass gate 99 at pin terminal (26). These ninety-nine 3-microsecond pulses are used in the final output gating.

The first interval, between pulses 1 and 2 of the 99 pulses, is used for reading 1/50 second. The pulse provided is gate 1/50 second at pin terminal (8). During the second interval, between pulses 2 and 3, seconds are read by means of the gate-seconds pulse at pin terminal (7). The third interval is used to generate the gate-minutes pulse at pin terminal (6), which allows minutes to be read.

During intervals 4 and 5, the data of channel 1 is read from the memory. Simultaneously with pulse 6, there occurs the 31-kilohertz shift-pulse at pin terminal (10), which shifts the data into the memory system by one element, so that the data of channel 2 is now in position to be read. Reading occurs during intervals 6 and 7. The 31-kilohertz gate pulse at pin terminal (19) gates the data of a particular channel so it is placed in adjacent characters. See the tape format description (Figure 7).

In the case of the optional 102 character format, the F/3 (+) pulse is delayed in reaching Card 8. Card 15 gates three 62-kilohertz pulses. Following these three pulses, the F/3 (+) delayed-pulse initiates the operation of Card 8 as usual.

Holding Register and Gates Card 1/50 Second Count (Card 9)

The 36-bit time code input at pin terminal (29) has 100 pulses per second. These are divided by two, and then counted in a binary fashion to yield 1/50 second. The counting procedure is then reset, with the 1 PPS pulse at pin terminal (27). See Figure 23. The binary counter is read by the read 1/50-second pulse at pin terminal (30) at a time when it is not changing, and the accumulated number is held in a flip-flop holding-register. The gate 1/50-second pulse at pin terminal (7), from the master timing card, reads the holding register at the correct time.

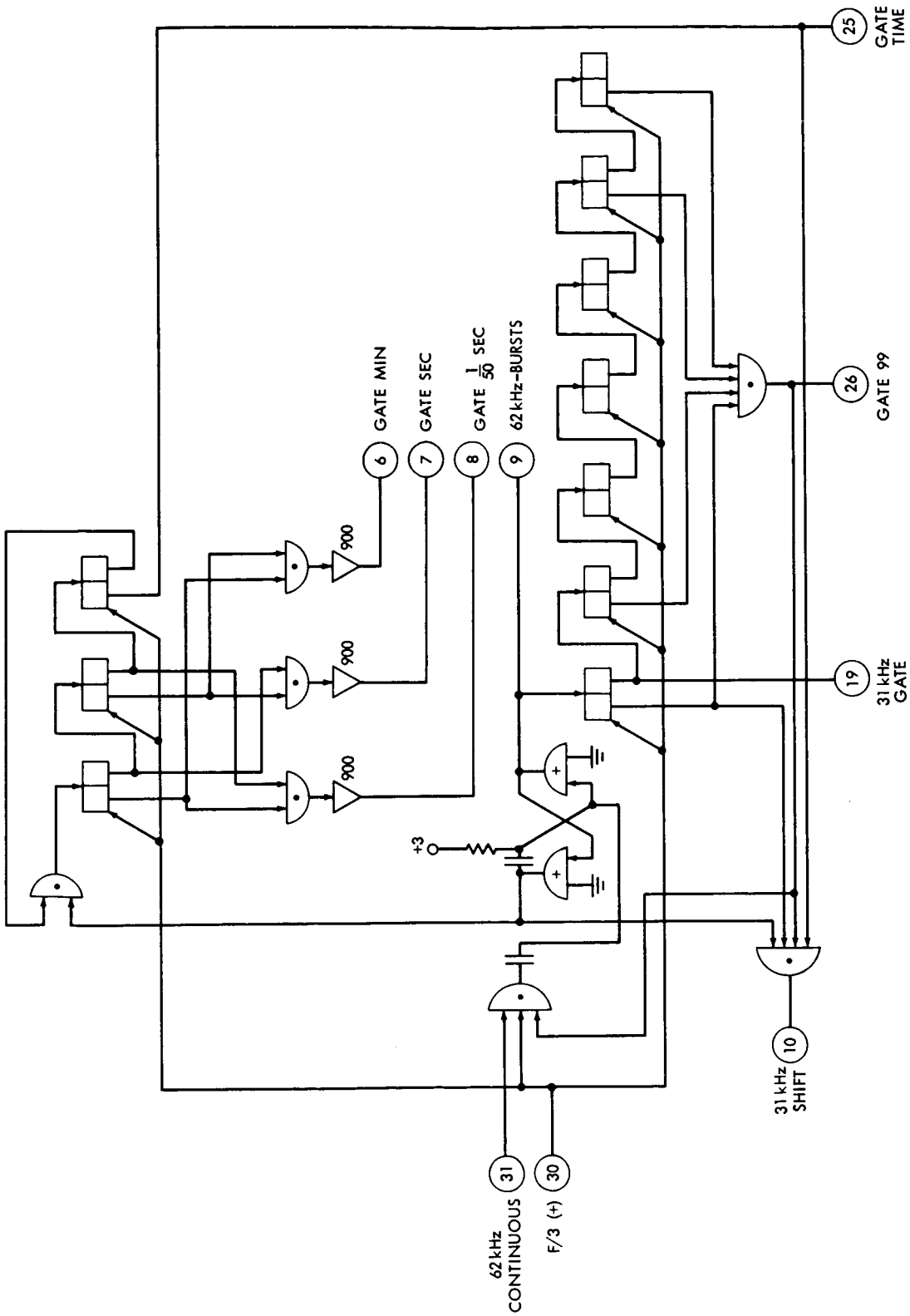


Figure 21. Master Timing Card 8, Logic Diagram

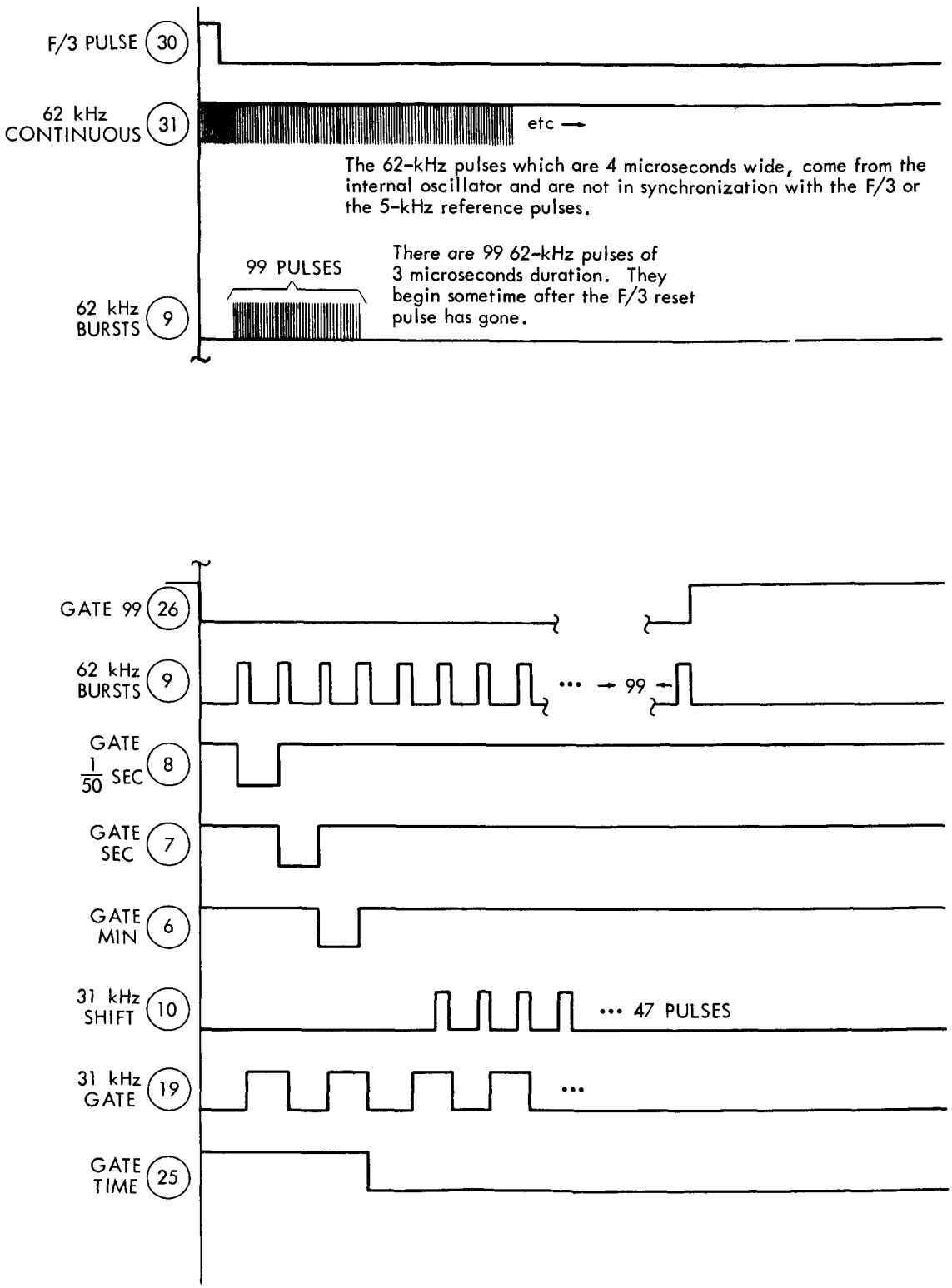


Figure 22. Master Timing Card 8, Waveforms

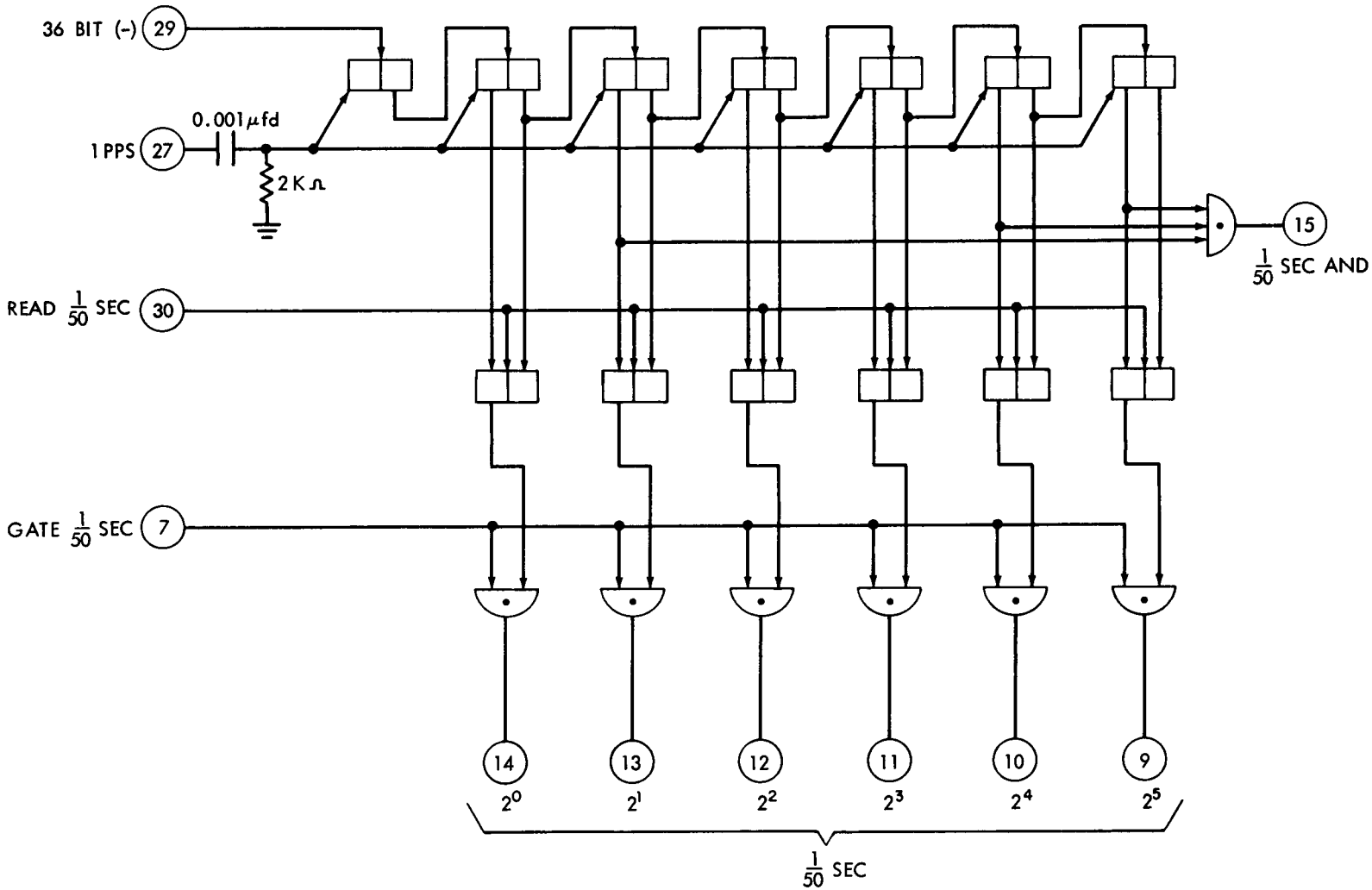


Figure 23. 1/50 Second Count, Holding Register, and Gates Card 9, Logic Diagram

The outputs of certain counting-register flip-flops are gated to provide the 1/50-second AND output at pin terminal (15), which is used to generate the 1 PPS pulse. Initially, a pulse from the 1 PPS generator card resets the 1/50-second counter. This reset pulse occurs approximately 4 milliseconds after the beginning of a new time frame. The 1/50-second AND occurs exactly at the beginning of the time frame. The AND is sensed by the 1 PPS generator card, now producing a reset pulse which occurs exactly at zero. The 1/50-second counters are then reset. Thus, when the circuit is working, the 1/50-second AND lasts only nanoseconds, and it is difficult to see on an oscilloscope.

Longitudinal Parity Card (Card 10)

Card 10 examines all data lines, and prints a longitudinal parity bit at the end of a data-block in each channel which contains an odd number of bits (Figure 24).

The F/3 (+) pulse, at pin terminal (31), resets the flip-flops before each data block. The flip-flops reverse the state (toggle) on each 1 bit, and hold the count. The 99-gated signal goes positive at the end of the data block and fires a 50-microsecond one-shot multivibrator, which then fires a 0.75 microsecond one-shot multivibrator to examine the states of the counter flip-flops, and to print the proper parity character. During this sequence NL input-signal at pin terminal (14) is low and NH input-signal at pin terminal (15) is high. These signals come from start-stop Card 1. Groups I and II of the OR gates are grounded through 2 transistors. These 2 transistors are controlled by stop-start Card 1, and are saturated during normal operation.

When the Data Format Converter is turned to OFF, the transistors of Groups I and II are conditioned so that nothing can be printed between the last longitudinal parity and the end-of-file. The transistor of Group II is again saturated during the end-of-file marker, to provide ground.

The longitudinal parity Card 10 circuit examines all 7 channels of the output format. The lateral parity bit of the longitudinal parity character is therefore determined by this card, and not by the lateral parity generator. It does not necessarily contain an odd number of bits.

Output Timing and Final Output Gates (Card 11)

Card 11 provides output-timing pulses at a time when no information is changing. Output lines 1, 2, 4, 8, A, B, and P are gated by the same output-timing pulse at pin terminal (30) to avoid any skewing of information. See Figures 25 and 26.

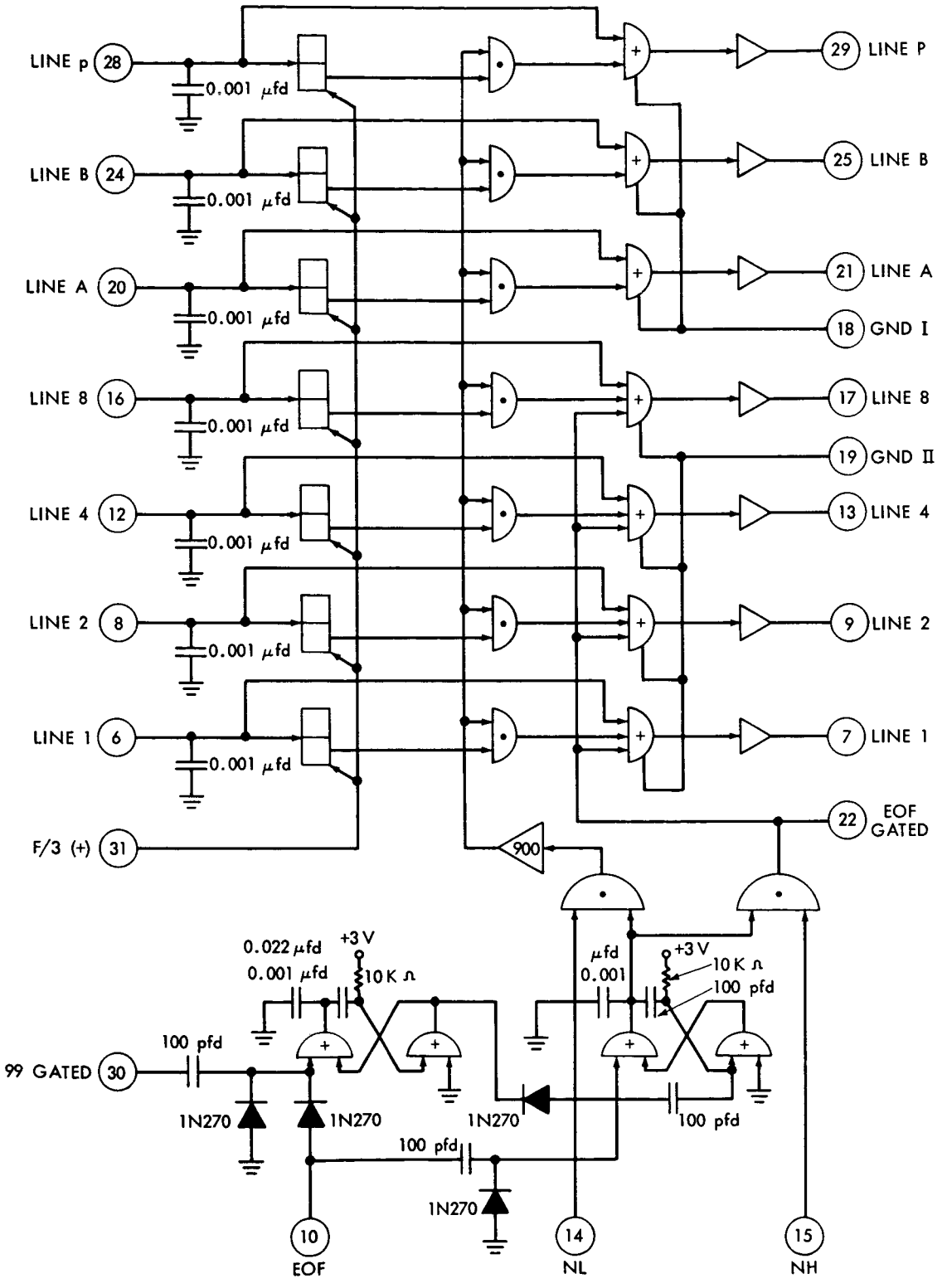


Figure 24. Longitudinal Parity Card 10, Logic Diagram

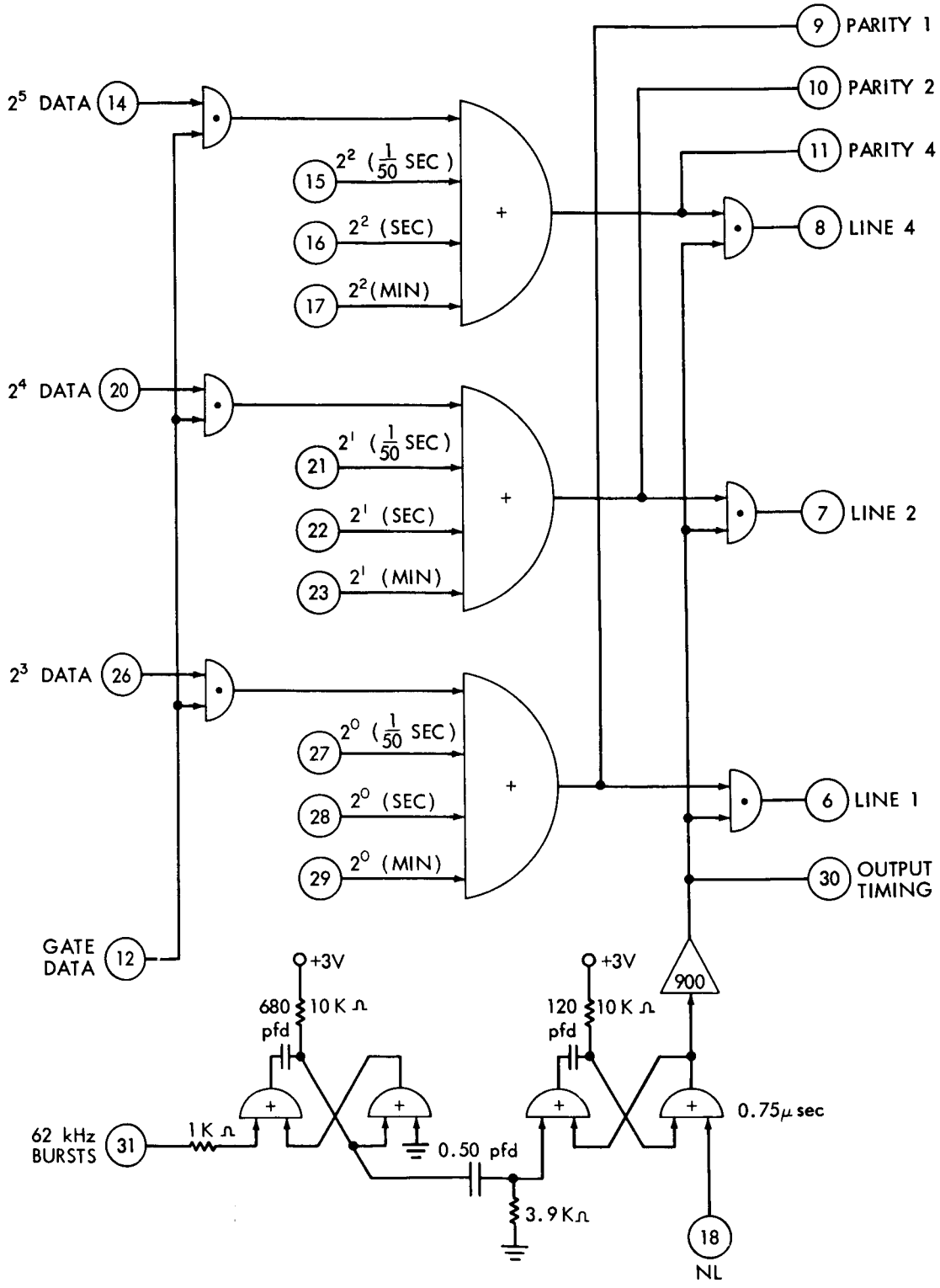


Figure 25. Output Timing and Final Output Gates Card 11, Logic Diagram

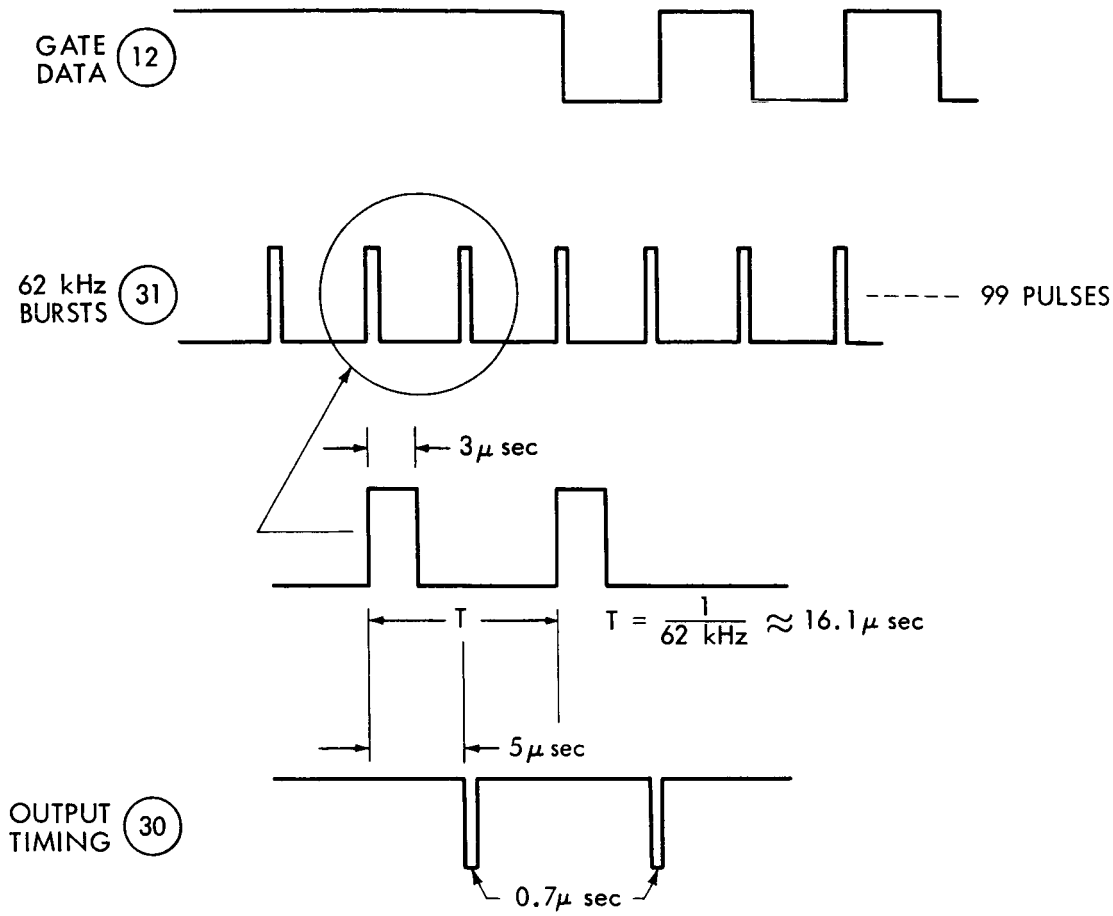


Figure 26. Output Timing and Final Output Gates Card 11, Waveforms

The 62-kilohertz pulse train is used to gate all data. These data are read by the output gates on this card, and on Card 12, 5 microseconds after a 62-kilohertz pulse, to ensure that no information is changed during gating. The output-timing pulses at pin terminal (30) are 0.75 microsecond. Two one-shot multivibrators on Card 11 provide both the 5-microsecond delay and the 0.75-microsecond gating pulses. The input signal NL at pin terminal (18) prevents any output-timing pulses from occurring before the Data Format Converter is turned to ON, or after it is turned to OFF, by disabling the 0.75-microsecond one-shot multivibrator.

Data Control and Final Output Gates (Card 12)

Final output gates for 4 channels, plus data gating control, are contained on Card 12 (Figures 27 and 28). Since 9 channels of data are to be read onto 6 output-channels, data reading must be staggered in time. (Refer to the description of tape format, Figure 7.) Data from one PPM channel appears in two

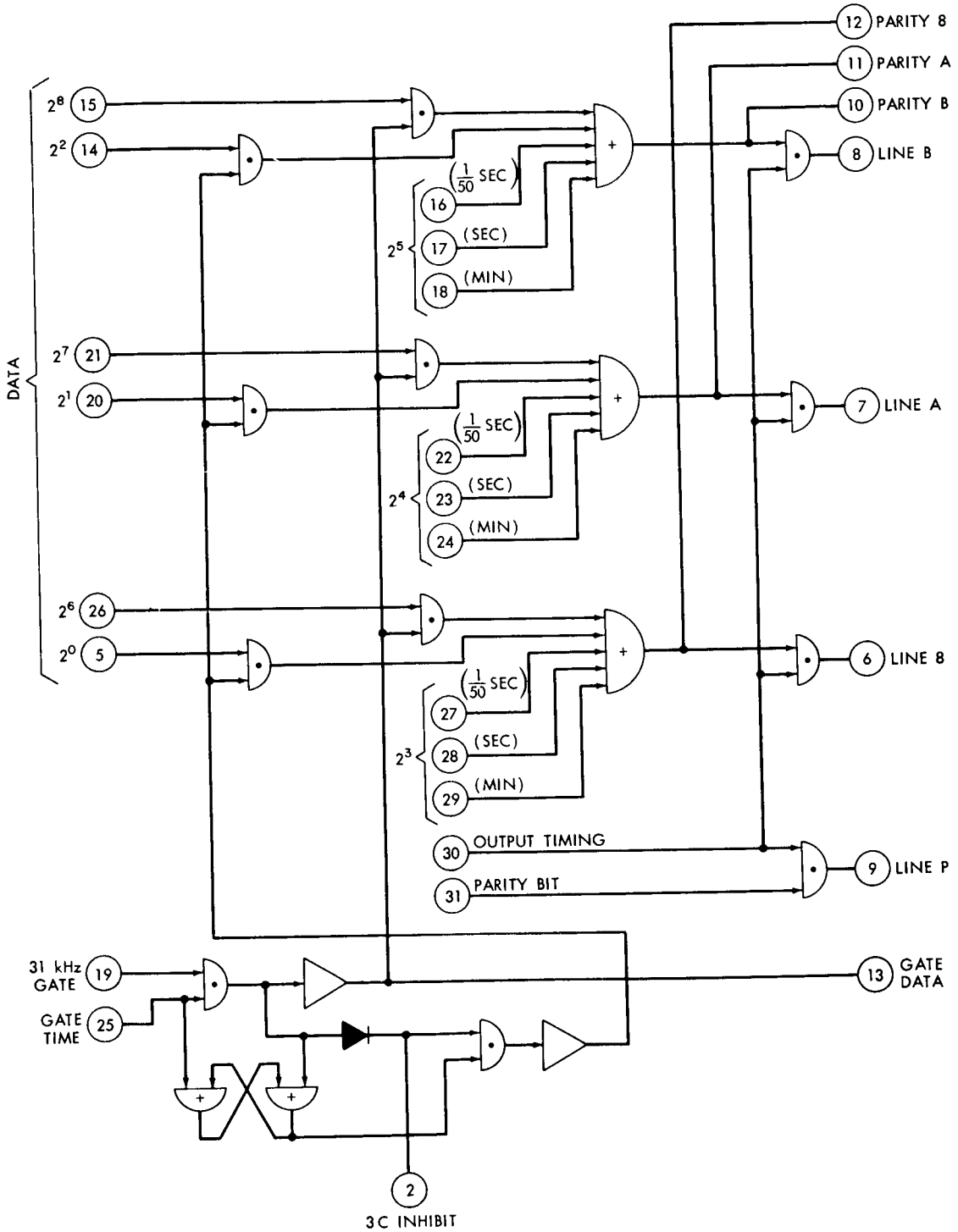


Figure 27. Data Control and Final Output Gates Card 12, Logic Diagram

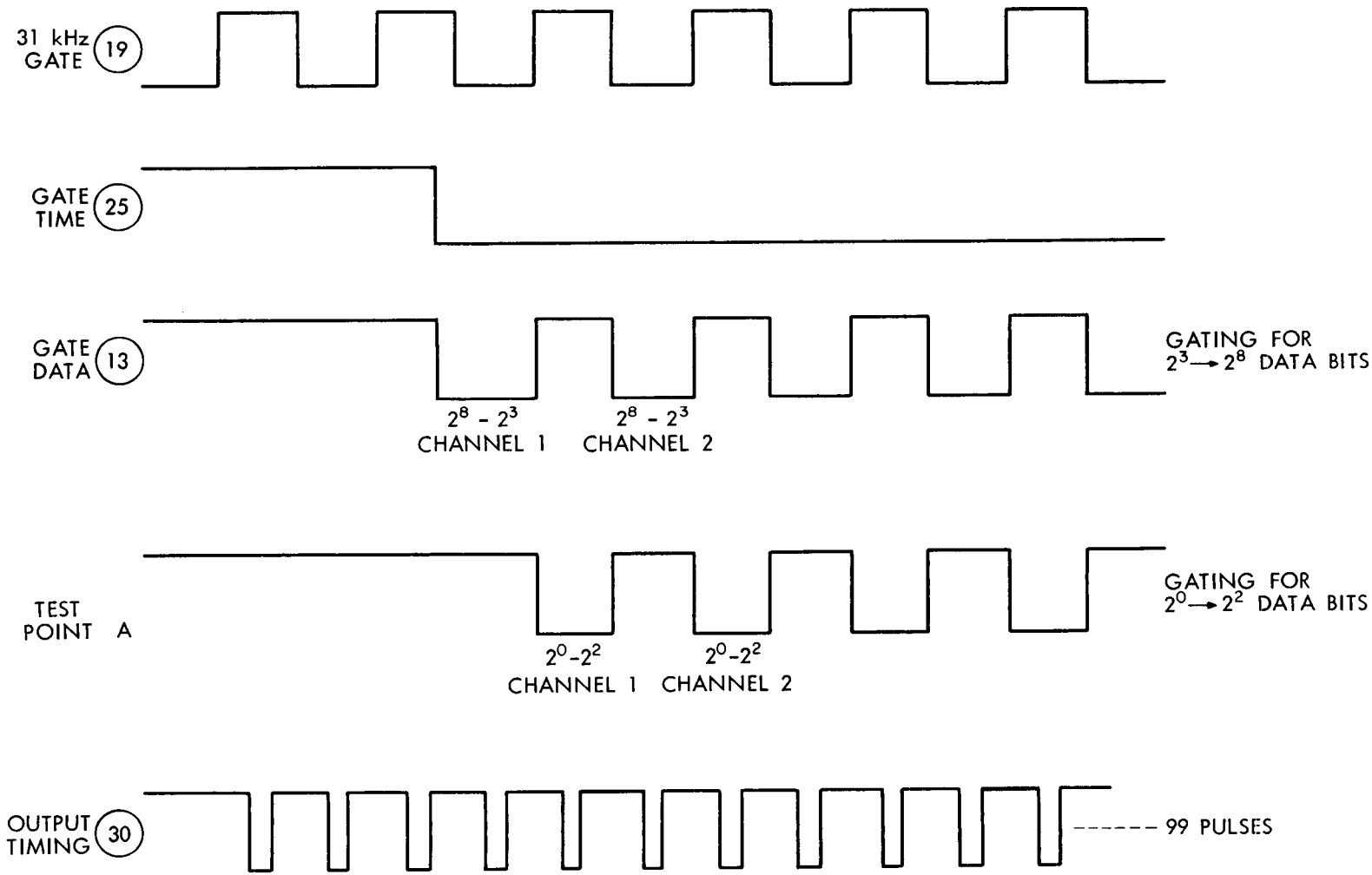


Figure 28. Data Control and Final Output Gates Card 12, Waveforms

magnetic tape characters. Data for the first character is gated by output gate data at pin terminal (13). Data in the second character is gated only on Card 12. Gating control appears at testpoint A (Figure 28). All inputs to a particular tape channel are collected in OR gates. The OR gate outputs are first transferred to the lateral parity generator (Card 13) and then back to the final output gates (Card 12).

Three extra characters can be added at the beginning of the 99-character record. (See Figure 7.) For these three characters to be blank (except for parity), an extra gating inhibit-input is needed, and the 3C inhibit (Card 12) at pin terminal (2), is used. The inhibit-input is not used when only the 99-character record output is desired.

Lateral Parity Card (Card 13)

Card 13 examines data output to output lines 1, 2, 4, 8, A, and B, and generates a 1 whenever there are an even number of 1's at the input lines. (See Figure 7.) Negative logic is used, and the output from the card appears in line 7 of the tape format. (See Figure 29.)

Memory Control Card (Card 14)

Card 14 provides the basic waveforms necessary for the operation of the Data Format Converter (Figures 30 and 31). The frame input at pin terminal (29) is reduced in repetition rate from 312 to 104 hertz. The F/3 output pulse at pin terminal (28) is the only output from this card which is necessary to check the operation of the Data Format Converter without using the memory system circuits.

The F/3 pulse provides synchronization for Card 14. Flip-flop I changes its state with the F/3 pulse, thus gating the data inputs to fill register 8A on one F/3 pulse, and to fill register 8B on the next F/3 pulse. The changes of state (toggle) inputs to fill-register 8A and to fill-register 8B (toggle inputs at pin terminals (6) and (7)) are controlled by the circuitry of Card 14. Card 14 also provides the 5-kilohertz reference pulse at pin terminal (30) for shifting data in, as well as the 31-kilohertz shift-pulses at pin terminal (31).

The leading edge of the ninth reference pulse, which changes the state of (toggles) flip-flop II, controls the toggled inputs to the 20-bit shift-registers at pin terminal (8). Between reference one and nine, registers 20-I and 20-II are shifting at a rate of 31-kilohertz. Data are being read on the ninth reference; flip-flop II reverses (changing the shift pulses which go to the first 20-bit register) to 5-kilohertz, to accept more data. Count 8 input at pin terminal (13) triggers a one-shot multivibrator on Card 15 which, after a delay of approximately

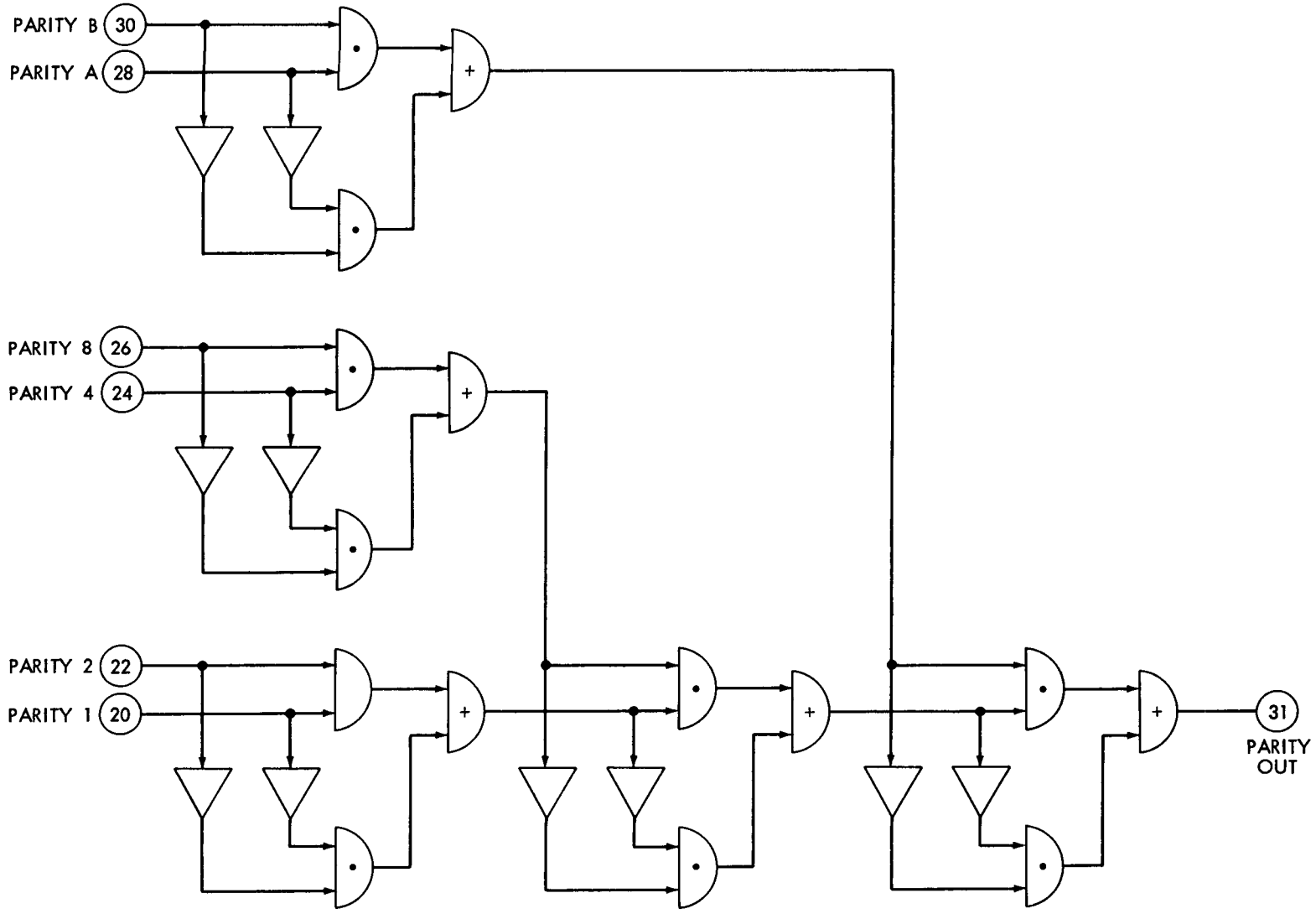


Figure 29. Lateral Parity Card 13, Logic Diagram

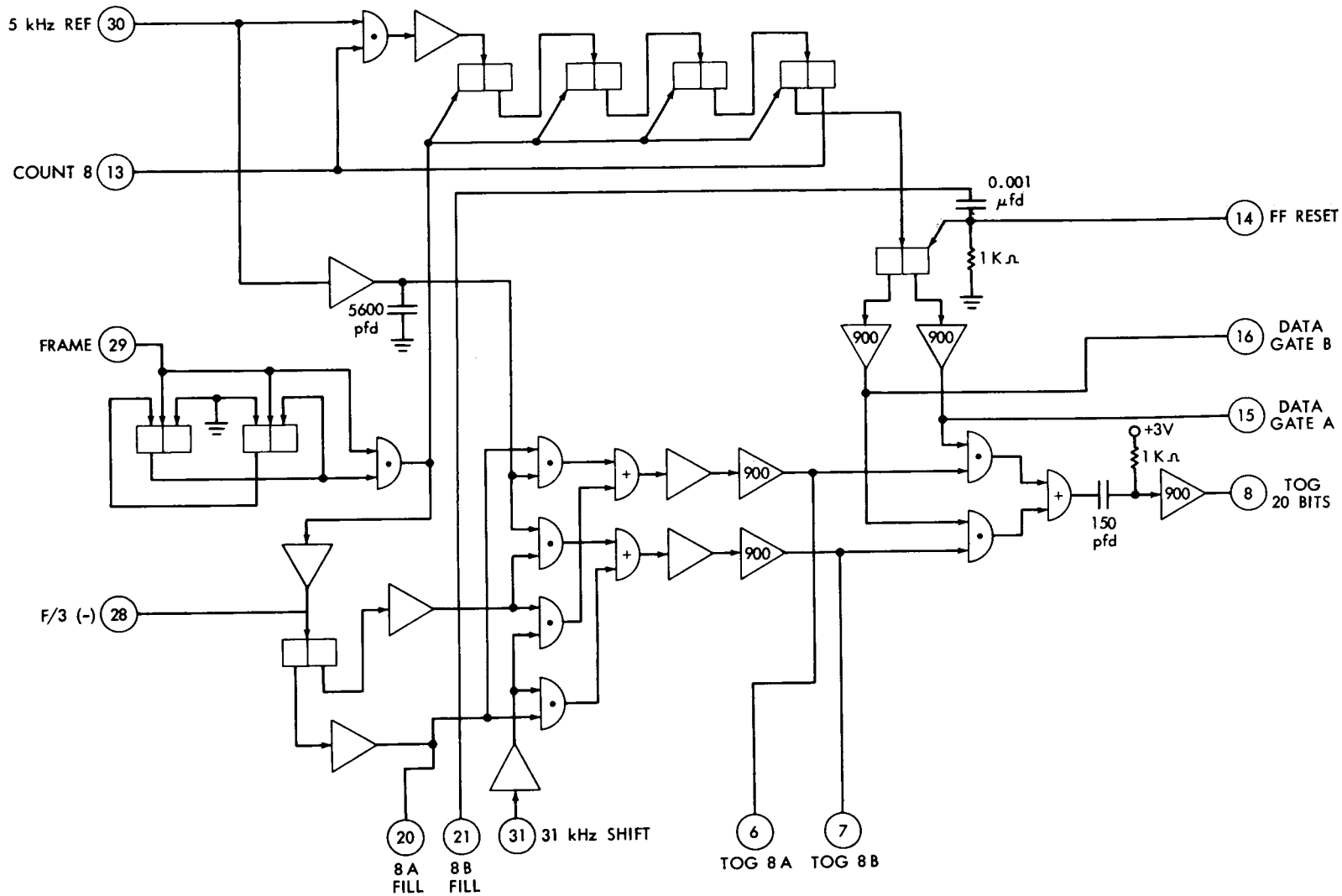
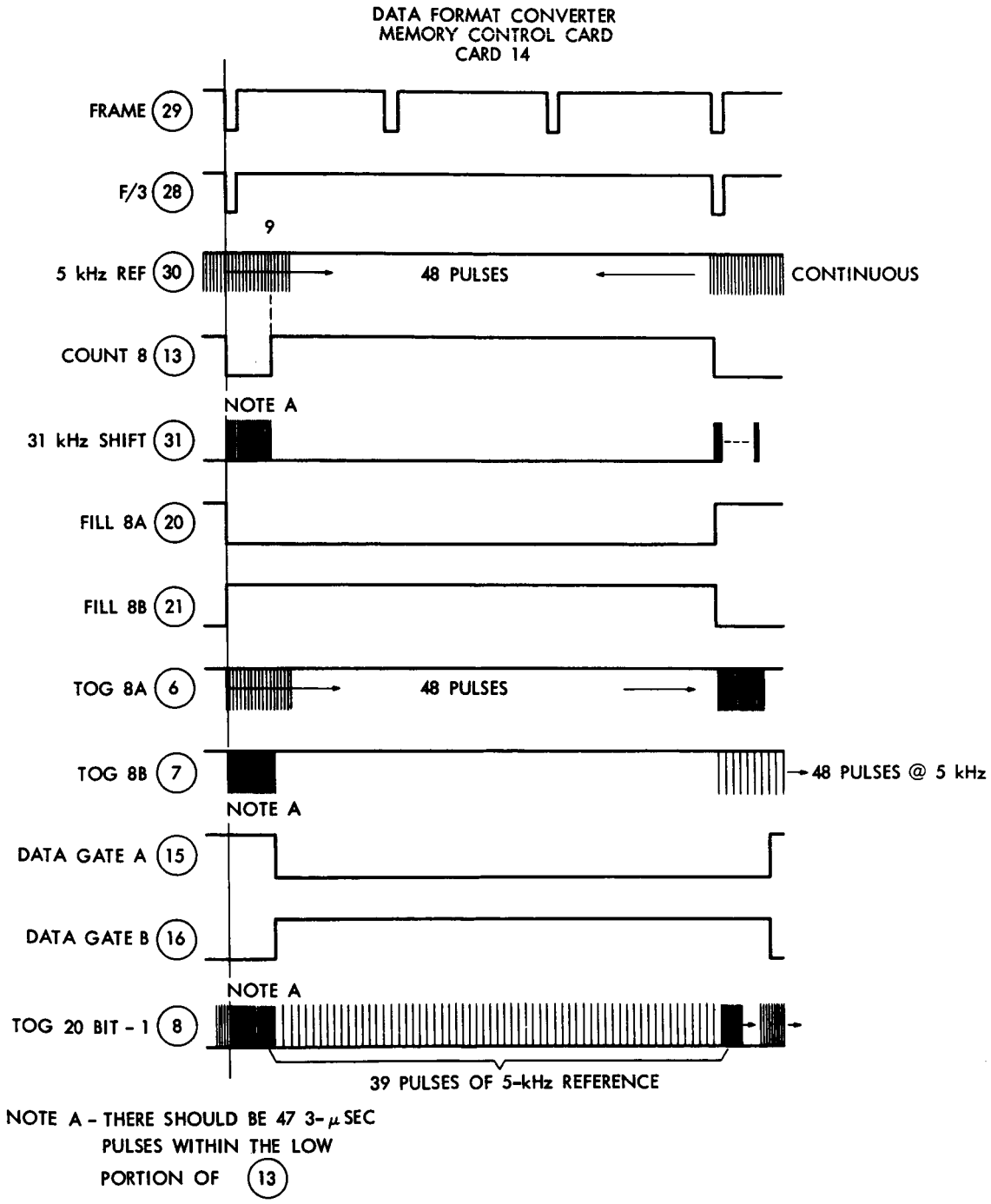


Figure 30. Memory Control Card 14, Logic Diagram



NOTE A - THERE SHOULD BE 47 3-μSEC PULSES WITHIN THE LOW PORTION OF (13)

Figure 31. Memory Control Card 14, Waveforms

1 millisecond, changes the state of the flip-flop on Card 15, changing the shift rate to the second 20-bit register back to 5-kilohertz. Synchronization between flip-flop II of Card 14 and the flip-flop on Card 15 is maintained by flip-flop reset 14. This slight delay for register 20-II is necessary to accommodate extra characters at the beginning of the original 99 character format.

Card 15 (Add Characters Card) or Card 15 Jumper

Card 15—Card 15 is included so that additional characters may be added to the original 99 character record. Currently, three extra blank (except for lateral parity) characters may be added to give a total of 102 characters (an even multiple of 6) for convenience in Fortran programming. See Figures 32 and 33.

The Data Format Converter wiring system is such that the F/3 pulse enters Card 15 before going to the master timing card. If three characters are to be added, the F/3 pulse is delayed until two 62-kilohertz pulses are counted. Then, the F/3 delayed pulse at pin terminal (30) is produced, initiating other functions of the system. A third 62-kilohertz pulse is then produced. Together, the three 62-kilohertz pulses perform an OR function, before the ninety-nine 62-kilohertz pulses are produced by the master timing card (Card 8), thus providing space for 102 characters. The 3C input pulse at pin terminal (2) is necessary to inhibit data-gating in Cards 11 and 12, in order that the extra three characters may be blank. Parity generation is not changed with the addition of the three characters, therefore, the extra three characters contain only a lateral parity bit.

In addition, Card 15 contains circuitry to provide the gating for the reverse-state (toggle) pulses to all 20-II registers of the memory system. See the data memory subsystem explanation (Page 6) for details of the function of this additional circuitry.

Card 15 Jumper—If the additional three characters generated by Card 15 are not desired, Card 15 jumper must be used. See Figure 34. When the jumper card is in place, the ninety-nine 62-kilohertz pulses at pin terminal (9) are connected to pin terminal (24), while the F/3 pulses at pin terminal (26) are connected to pin terminal (30), thus bypassing the normal configurations. The jumper card also contains circuitry to provide change of state (toggle) pulses to the 20-II registers of the memory system. Both Card 15 and Card 15 Jumper contain a double inverter circuit (through which input pulse 20-I passes) to delay this signal. This delay ensures that the change of state (toggle) pulses to 20-II occur before those to 20-I, thus also ensuring that no data is lost when shifting from 20-I to 20-II.

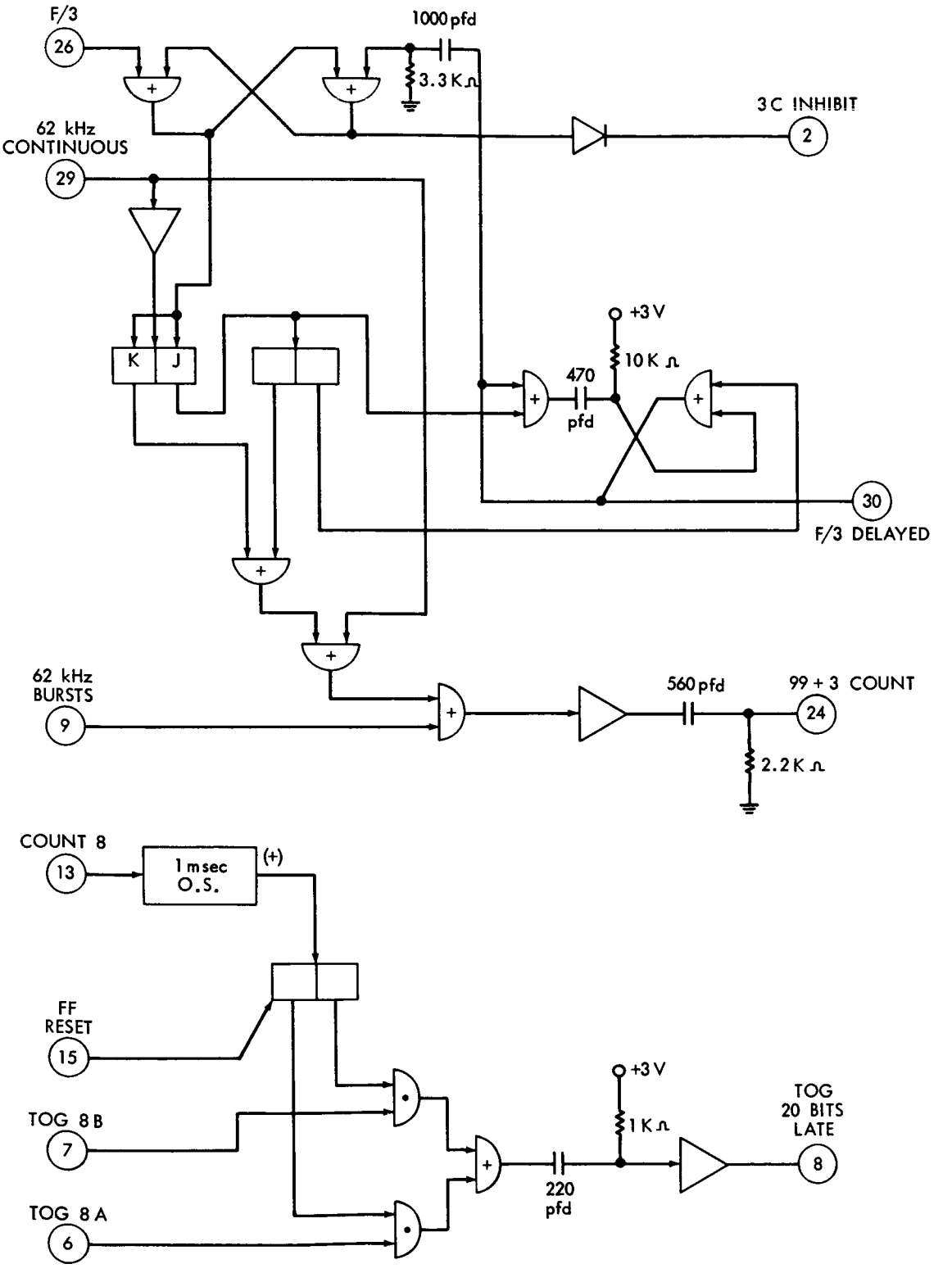


Figure 32. Add 3C Card 15, Logic Diagram

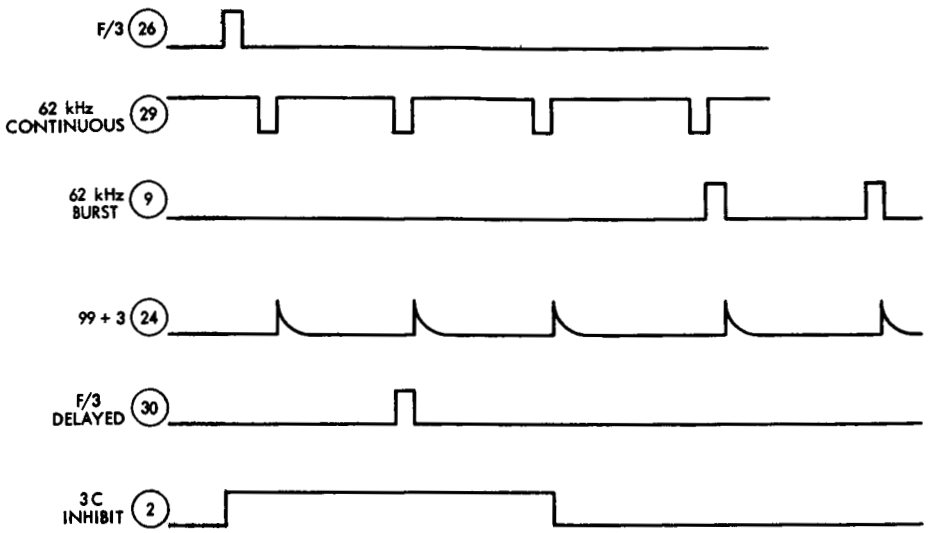


Figure 33. Add 3C Card 15, Waveforms

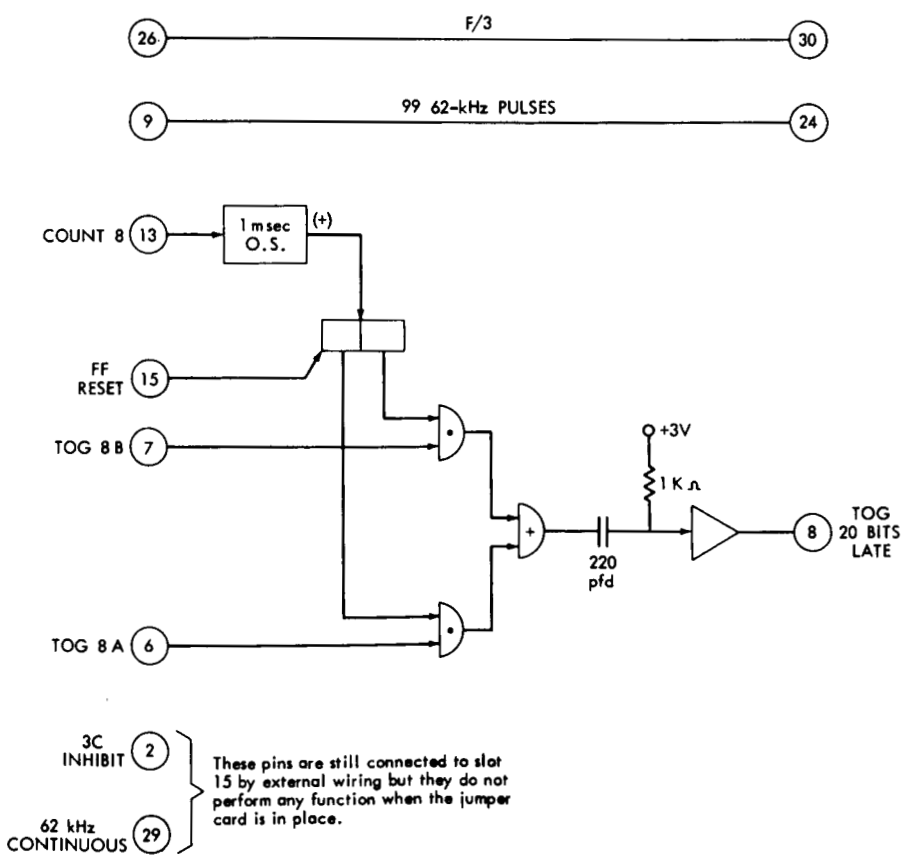


Figure 34. Card 15 Jumper, Logic Diagram

Output Driver Card (Card 16)

Card 16 is necessary when the Data Format Converter is used with the CEC DR-3000 data tape unit, using positive logic (Figure 35). The output driver, as shown, produces a zero to +10 volt output, from a zero to +3 volt input signal. There are seven identical circuits on the card to handle seven input lines. If a different tape unit is used, Card 16 should be altered to meet its particular input requirement.

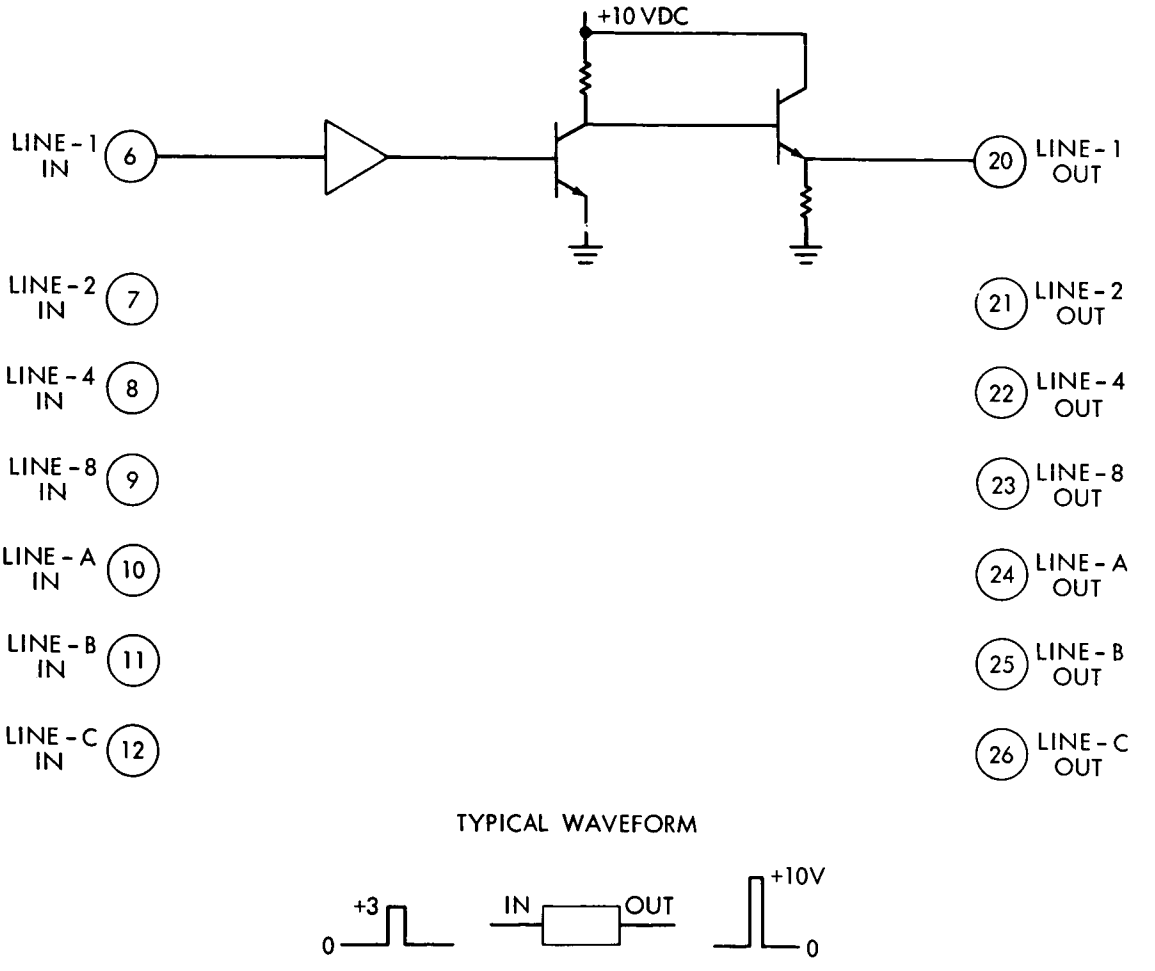


Figure 35. Output Driver Card 16, Logic Diagram